Nickel/Copper Plated Contacts as an Alternative to Silver Screen Printing for the Front Side Metallization of Industrial High Efficiency Silicon Solar Cells

Loic TOUS

Jury:
Prof. dr. ir. P. Van Houtte, chair
Prof. dr. ir. R. Mertens, supervisor
Prof. dr. ir. J. Poortmans, supervisor
Prof. dr. ir. J. Driesen
Prof. dr. ir. J. Vleugels
Prof. dr. ir. W. Sinke
(ECN Solar Energy, Netherlands)
Dr. T.M. Bruton
(TMB Consulting, UK)
Mr. R. Russell (imec)

Dissertation presented in the partial fulfillment of the requirements for the degree of Doctor in Engineering

In collaboration with

Kapeldreef 75,
B-3001, Heverlee (Belgium)

January 2014

D/2014/7515/12
ISBN 978-94-6018-788-9

Acknowledgements

Writing acknowledgements remembers me of the first months into my PhD thesis, I had plenty of ideas but I did not know what to start with. I also did not know that both my PhD topic and the persons guiding me would change several times during my first few years at imec due to numerous organizational changes. Although these changes required some adaptation, they also gave me the opportunity to broaden my know-how and to strengthen bonds with both existing and former colleagues.

The person that opened me to the door to imec via a Master's thesis and tirelessly worked in maintaining close collaboration within the i-PERC team is Joachim John and for that I am very grateful. Thank you for your constant support and encouragements, it truly made life at imec and outside imec more fun. In the same vein, I am very thankful to Christophe Allebe for bringing me along in the lab and pushing me towards doing a PhD thesis at imec. You always showed an extraordinary positive attitude and it really was a great pleasure to work under you supervision even if this was for a short period of time. If Christophe pushed me towards doing a PhD thesis, it was my promoters Prof. Robert Mertens and Prof. Jef Poortmans together with our former group-leader Emmanuel Van Kerschaver who gave me this possibility. I particularly want to thank Robert and Jef for their critical feedback during our monthly follow-up meetings, for their great help with writing this manuscript, and more importantly for making research in PV possible at imec.

I am very thankful to the members of my PhD examination committee: Prof. Paul Van Houtte, Prof. Jozef Vleugels, Prof. Wim Sinke, Dr. Tim. M. Bruton, and Richard Russell. Thanks a lot for your suggestions which greatly contributed to improve the quality of this manuscript.

As starting a PhD requires solid background knowledge, I would also like to thank my professors at INSA (Lyon, France) for providing me with fundamental and practical knowledge in a broad number of topics.

I would like to express my gratitude to everyone at imec as well as industrial partners for making it possible to perform research using state-of-the-art research facilities as this requires a very talented group of students, technicians, operators, engineers, scientists, and managers as well as a strong financial support. I would like to thank master students present during my Master's thesis at imec who early-on helped me discovers the joys of living in Belgium (Sylvain, Tuomas, Michael, Frederic, Luca, Vladimir, and many more). That together with the amazing display of skills of PhD students within the PV group definitely contributed to me choosing to stay at imec for a PhD. Thanks to Chun, Bart, Victor, Emanuele, Rufi, Alex, Angel and more recently to Hari, Stefano, Roberto, Hans, Christos, Jan, Chi, Brett for teaching me how to design experiments, get them moving, prepare joint-papers/presentations, and share the fun during conferences! Thanks as well to my master students Claudia Lo Presti and Alireza Rouhi for their great help. I would like to thank the members of the PV team with whom I work more closely; namely Jose-Luis (for taking over Christophe for a while as my daily supervisor); Patrick, Tom, Erik (for helping out with diffusions/oxidations/PECVD depositions); Jo (for laser experiments);

Riet, Sukhvinder, Maria, Iza, Anne, Aude, Ronald, Jo, Xavier (for helping out with various stages of processing); Maarten (for all the great help with PV characterization tools); Michael (for the amazing support with all wet-processing tools); and Koen, Antonios, Monica (for the help with simulations). It has been (it is) a great pleasure to work with you and I am very proud of the results we have achieved together during these past 4 years. My profound gratitude goes to the people from support & operations as without them there wouldn't be a single tool up and running at imec, and god knows how often these tools moved-in/out or broke down. So thanks to Andre, Stefan, Didier, Dirk, Geert, Reinoud, Kristof, Luc, Jeroen for working crazy-hours and for always doing your best. A special thanks goes to Giovanni, Ivan, and Francis for solving every kind of hardware, organizational, logistic problem. I am also grateful to experts from imec who helped me with various aspects of characterization or device integration. Hugo Bender and Chris Drijbooms for TEM/FIB, Karl Opsomer and Jorge Kittl for *in-situ* XRD, Johan Meersschaut for RBS/ERD, Alain Moussa for AFM, Bastien Douhard for SIMS, and Tobias Pletzer (from TU Aachen) for SR/Reflectance measurements. I also want to thank people from the FPS group who helped me with plating (Harold Philipsen, Mia Honore, Simon Rodet, Kevin Vandersmissen) or with sputtering (Sander Van Gompel). I am particularly thankful to Dennis van Dorp for setting up both electroless and light-induced Ni plating baths.

I am deeply grateful to Jörg Horzel for bringing to imec focus, years of experience in research and manufacturing of industrial silicon solar cells, and the passion to push limits relentlessly. I learned enormously from you and I believe that it is greatly thanks to you that the entire group made such fast progress in recent years. Thank you! For the same reasons, I would like to thank Jozef Szlufcik and Filip Duerinckx for whom I have profound admiration and with whom it is great pleasure to work with.

As being at imec gave me the great opportunity to work closely with equipment suppliers, I would like to thank them for the strong and very productive collaborations. From MECO, I would like to thank Jurgen Bertens, Johan Beckers, Martijn Zwegers, Ed Vervoort, Lucas van den Brekel and many more. It is a pleasure to work with you guys and I am very much looking forward to what we will be doing next! For the same reasons, I would like to thank Thierry Emeraud, Jean-Francois Lerat, Karim Huet, and Razvan Negru from EXCICO.

Lastly I want to thank a select number of people that were absolutely essential to me. I am forever grateful to my family for its support and for teaching me what matters in life. Thanks to many of my friends here in Belgium and elsewhere for encouraging me and for keeping me out of the lab; be it for going-out, playing squash, or traveling. Thank you Richard for being not only an excellent supervisor but also a good friend. I am truly amazed by how much progress we have made together with Ni/Cu plated contacts in the last couple years and by how much I still have to learn from you in terms of critical thinking and experimental planning. Thanks for your guidance, thanks for your British humor and sarcasms, and I hope we will keep climbing mountains together. As a final word, I would like to thank Suzanne who has made be truly happy ever since an evening in August 2010. Thanks for your patience and for giving me so much love.

Abstract

Nickel/copper plated contacts as an alternative to silver screen printing for the front side metallization of industrial high efficiency silicon solar cells.

Solar power generation is largely dominated by photovoltaic (PV) systems which directly convert the incident sun irradiation into electricity. While rapidly declining prices are opening new opportunities for PV, further reductions in manufacturing costs are essential as nearly all PV manufacturers (wafer, cell, modules) experienced losses in 2012. As most of a PV system cost is area related, the highest impact on cost can be achieved by increasing the efficiency of the solar cells in the PV modules while reducing manufacturing costs. This thesis aims at replacing conventional silver (Ag) screen printed (SP) front side contacts by nickel/copper (Ni/Cu) plated contacts in industrial high efficiency silicon solar cells. It is motivated not only by the limitations that SP-Ag front side contacts have regarding solar cell efficiencies (high shading losses, limited line conductivity, and poor contact resistance to moderately doped junctions), but also by the PV industry's desire to reduce Ag usage to below 50 mg/cell for cost reasons by 2017.

Despite the potential advantages of Ni/Cu contacts, their commercialization has so far been limited with the notable exception of BP Solar between the years 1992 and 2008. Reasons for the limitation include the increased process complexity, the availability of suitable low-cost production techniques/tools at that time, and doubts over the cost advantage and long-term reliability. To address these issues, a relatively simple process sequence to define self-aligned Ni/Cu plated front contacts has been developed in this thesis which required to clarify the interactions between front emitter profile, front dielectric(s) patterning, metal deposition, and nickel silicidation. High average solar cell efficiencies ~20.5% (109 cells) with a tight distribution were obtained when applying this sequence to 156x156 mm^2 p-type PERC cells and using more industrial plating techniques/tools that were not available to earlier Ni/Cu adopters like BP Solar. First PV modules made from similar cells passed 1.5x thermal cycling and damp heat testing as defined in IEC61215 and accelerated thermal ageing tests indicated that long-term reliability (25+ years at 85˚C) is feasible. The cost to define Ni/Cu plated contacts with this sequence was calculated to be ~4.4€c/cell cheaper than the one for SP-Ag contacts which makes it one of the few technologies that can improve both the efficiency and the cost per cell of the technology it aims to replace.

In parallel, Ni/Cu plated contacts were applied to rear emitter n-type PERT cells and a novel silicidation technique based on excimer laser annealing (ELA) was investigated. For the former, efficiencies up to 20.5% were demonstrated in a first trial and a power-loss analysis was conducted which confirmed their higher efficiency potential compared to p-type PERC cells. Even more promising results were obtained when applying ELA to hybrid n-type PERT cells based on a heterojunction rear emitter.

Beknopte samenvatting

Elektrochemisch gedeponeerde nikkel/koper contacten als alternatief voor zilver zeefdruk voor metallisatie van de voorzijde van hoog-efficiënte industriële silicium zonnecellen.

De opwekking van zonne-energie wordt gedomineerd door fotovoltaïsche systemen (PV) die zonlicht direct converteren naar elektriciteit. Ondanks de snelle daling van prijzen voor PV systemen, is een verdere reductie van productiekosten noodzakelijk om de financiële toestand van de PV fabrikanten van substraten, cellen en panelen te verbeteren. Aangezien het grootste deel van de kosten van PV systemen oppervlakte gerelateerd is, kan de hoogste impact op deze kosten gerealiseerd worden door het verhogen van de efficiëntie van de zonnecellen in de PV panelen tezamen met een daling van de productiekosten. Het doel van deze thesis is om de conventionele zilver (Ag) zeefdruk (SP) contacten op de voorzijde van industriële silicium zonnecellen te vervangen door elektrochemisch aangebrachte nikkel/koper (Ni/Cu) contacten. De motivatie hierachter is niet alleen de beperkingen die SP-Ag voorzijde contacten hebben met betrekking tot efficiëntie (hoge schaduwverliezen, beperkte geleidbaarheid en hoge contactweestand voor laag gedopeerde emitters) weg te werken, maar ook het zilvergebruik te beperken tot maximaal 50 mg/cel tegen 2017 omwille van de kostprijs van het metaal.

Ondanks de potentiële voordelen van Ni/Cu contacten is de commercialisering nog eerder beperkt, met uitzondering van de panelen geproduceerd door BP Solar tussen 1992 en 2008. De redenen voor deze beperking zijn het meer complexe proces, het ontbreken van goedkope productietechnieken/systemen en onzekerheid over het kostenplaatje en lange termijn betrouwbaarheid. Om deze problemen aan te pakken hebben we in deze thesis een relatief simpel productieproces ontwikkeld voor elektrochemisch gedeponeerde en gealigneerde Ni/Cu contacten. Hiervoor was het nodig de interacties tussen het doperingsprofiel van de emitter, het patroon van de laser ablatie van de diëlektrische lagen, de depositie van de metaallagen en finaal de sintering leidend tot nikkel silicidatie te onderzoeken en te beschrijven. Toepassing van het nieuwe ontwikkelde celproces heeft geleid tot een hoog gemiddeld rendement van 20.5% (109 p-type PERC cellen op 156x156 mm^2 monokristallijne silicium substraten) met een lage spreiding. Hierbij werd gebruik gemaakt van meer industriële metallisatie technieken/systemen die niet beschikbaar waren voor vroegere Ni/Cu adopters zoals BP Solar. De eerste PV-modules gemaakt met dergelijke cellen zijn onderworpen aan thermische cycli, aan vocht/warmte testen, (beide 1.5x zo streng als gedefinieerd in IEC61215) en aan versnelde thermische verouderingstesten. Deze geven aan dat betrouwbaarheid op lange termijn (25+ jaar bij 85˚C) haalbaar is. Een kostenberekening voor het aanbrengen van de Ni/Cu contacten resulteerde in een kostenbesparing van ~4.4 €c/cel in vergelijking met gezeefdrukte Ag contacten. Dit maakt dat deze technologie één van de weinige is die zowel het rendement als de kosten kan verbeteren in vergelijking met de technologie die ze beoogt te vervangen.

Parallel hieraan werden de Ni/Cu contacten aangebracht op de voorzijde van n-type PERT cellen met een achterzijde emitter en een nieuwe silicidatie techniek gebaseerd op excimer laser annealing (ELA) werd onderzocht. Voor de eerste technologie kon een rendement tot 20.5% behaald worden. Een vermogensverlies analyse bevestigde het hogere potentieel van dit soort cellen t.o.v. p-type PERC cellen. Nog meer veelbelovende resultaten werden verkregen bij toepassing van ELA op hybride n-type PERT cellen gebaseerd op een heterojunctie achterzijde emitter.

List of acronyms

acronym	description
AC	alternative current
AFM	atomic force microscopy
Al-BSF	aluminum back surface field
AM1.5g	air mass1.5 global spectrum
APCVD	atmospheric pressure chemical vapor deposition
ARC	anti-reflection coating
ASP	average selling price
CAPEX	capital expenditures
CBKR	Cross Bride Kelvin Resistor
CMOS	complementary metal oxide semiconductor
CoO	Cost of Ownership
CTE	coefficient of thermal expansion
CZ	monocrystalline silicon produced with Czochralski method
DARC	double anti-reflection coating
DC	direct current
DH	damp heat
DIW	de-ionized water
DOE	design of experiment
ECA	electrically conductive adhesive
ED	energy density
EDS	energy dispersive X-ray spectroscopy
EELS	electron energy loss spectroscopy
ELA	excimer laser annealing
EQE	external quantum efficiency
ERD	elastic recoil detection
EVA	ethylene vinyl acetate
FCA	free carrier absorption
FE	field emission
FGA	forming gas annealing
FIB	focused ion beam
FSF	front surface field
FSRV	effective front surface recombination velocity
FZ	monocrystalline silicon produced with float-zone method
HAADF	high-angle annular dark-field imaging
HF	humidity freeze
HF	Hydrofluoric acid
IBC	interdigitated back contact
IC	integrated circuits
IEC61215	international electrotechnical committee standard 61215
IHP	inner Helmholtz plane
ILD	inter layer dielectrics

acronym	description
IPCC	intergovernmental panel on climate change
i-PERC	industrial passivated emitter and rear cell
IQE	internal quantum efficiency
IR	infra-red
ITO	indium tin oxide
ITRPV	International Technology Roadmap for Photovoltaic
I-V	current voltage
LA	laser ablation
LBSF	local back surface field
LCMD	laser chemical metal deposition
LCOE	levelized cost of electricity
LDSE	laser doped selective emitter
LED	light emitting diode
LFC	laser fired contacts
LGBC	laser grooved buried contact
LID	light induced degradation
LIP	light induced plating
LMS	laser micro sintering
LTA	laser thermal annealing
LTC	laser transferred contacts
m-CZ	CZ-Si pulled with magnetic confinement
MIS	metal-insulator-semiconductor
m-Si	multicrystalline silicon
NHE	normal hydrogen electrode
OHP	outer Helmholtz plane
PECVD	plasma enhanced chemical vapor deposition
PERC	passivated emitter and rear cell
PERL	passivated emitter, rear locally diffused
PERT	passivated emitter, rear totally diffused
PL	photoluminescence
PSG	phosphorous silicate glass
PV	photovoltaic
PVD	physical vapor deposition
QSSPC	quasi-steady-state photoconductance
RBS	Rutherford backscattering
RH	relative humidity
ROI	Return On Investment
RSRV	effective rear surface recombination velocity
RTA	rapid thermal annealing
SALICIDE	self-aligned silicide
SBC	simplified buried contact
SCE	saturated calomel electrode
SCR	space charged region
SEM	scanning electron microscope

acronym	description
SHJ	silicon heterojunction
SIMS	secondary ion mass spectroscopy
SP	screen printed
SPM	sulfuric peroxide mixture
SRH	Shockley-Read-Hall
SRP	spreading resistance profiling
SSRM	scanning spreading resistance microscopy
STC	standard testing conditions
STEM	scanning transmission electron microscope
SWCT	smart wire contacting technology
TC	thermal cycling
TCO	transparent conductive oxide
TE	thermionic emission
TEM	transmission electron microscope
TFE	thermionic field emission
TLM	transfer length method
UV	ultra-violet
WE	wet-etched
XRD	X-ray diffraction
XRF	X-ray fluorescence

List of symbols

symbol	description	unit
$\Delta_{FS\text{-}RS}$	potential between front side and rear side	V
$\Delta_{RS\text{-}AUX}$	potential between rear side and auxiliary anode	V
a	length unit cell for 3, 5 or 15 busbars	m
A_{cell}	cell area	m^2
b	width unit cell II (see Chapter 4)	m
C_O, C_R	concentrations of oxidized and reduced species respectively	mol^{-1}
c_p	specific heat capacity	$J.kg^{-1}.K^{-1}$
D_{it}	interface trap density	$cm^{-2}.eV^{-1}$
d	contact spacing	m
E	energy level	eV
E_0	standard potential of Redox-couple	V
E_C	energy level of conduction band edge	eV
E_F	Fermi energy level	eV
E_{FB}	flat-band potential	V
E_G	energy band gap	eV
E_{redox}	electrochemical potential	V
E_V	energy level of valence band edge	eV
FF	fill factor	%
FF_0	maximum achievable fill factor	%
h	height/thickness	m
I	current	A
j	current density	$A.m^{-2}$
j_0	recombination current density	$A.m^{-2}$
j_{01}	recombination current density in emitter and base regions	$A.m^{-2}$
j_{02}	recombination current density in the space charge region	$A.m^{-2}$
j_{0b}	recombination current density in base	$A.m^{-2}$
j_{0e}	emitter dark saturation current density	$A.m^{-2}$
$j_{0e,\,met}$	emitter dark saturation current density in contact areas	$A.m^{-2}$
$j_{0e,\,pass}$	emitter dark saturation current density in passivated areas	$A.m^{-2}$
j_{mpp}	current density at maximum power point	$A.m^{-2}$
j_{ph}	photo-generated current density	$A.m^{-2}$
$j_{ph,nos}$	photo-generated current density without shading	$A.m^{-2}$
j_{sc}	short-circuit current density	$A.m^{-2}$
$j_{sc,max}$	maximum achievable short-circuit current density	$A.m^{-2}$
k	wave vector	m^{-1}
K	thermal conductivity	$W.m^{-1}.K^{-1}$
l_{bus}	busbar length	m^2
L_{eff}	effective diffusion length	m
l_f	finger length for 3, 5, or 15 busbars	m
L_t	transfer length	m

symbol	description	unit
l_{te}	length of tab extension	m^2
m	mass	kg
M	molar mass	$kg.mol^{-1}$
n, n_1, n_2	ideality factors	
N_{dop}	base doping	m^{-3}
N_s	dopant surface concentration	m^{-3}
N_{sb}	number of solder joints per busbar	
η	efficiency	%
O	oxidized metal species	
pFF	pseudo fill factor	%
P_{in}	power density of incident light	$W.m^{-2}$
P_{max}	maximum power output	W
P_{mpp}	power density at maximum power point	$W.m^{-2}$
Q	charge	C
r	area weighted resistance	$\Omega.m^2$
R	resistance	Ω
R_b	backside reflectance	%
R_{bb}	busbar to busbar resistance	Ω
R_c	contact resistance	Ω
R_t	total resistance	Ω
r_{dot}	effective rear contact radius	m
Red	reduced metal species	
R_{front}	front reflectance	%
r_p	parallel (or shunt) resistance	$\Omega.m^2$
r_s	series resistance	$\Omega.m^2$
R_{sh}	sheet resistance of a diffused region (emitter, FSF, BSF)	Ω/sq
s	finger separating distance (pitch)	m
s_{dot}	spacing between rear point contacts	m
T	absolute temperature	$^{\circ}K$
t	time	sec
t_f, t_b	transparency factor of fingers/busbars	%
T_m	melting point	K
V_{bi}	built-in voltage	V
V_{mpp}	voltage at maximum power point	V
V_{oc}	open-circuit voltage	V
v_{oc}	normalized open-circuit voltage	V
$V_{oc,max}$	maximum achievable open-circuit voltage	V
W	wafer thickness	m
w_{bus}, w_T	busbar width, tab width	m
w_c	contact width	m
Wp	watt peak	W
x_j	junction depth	m
z	number of electrons	
Z	contact length (only in appendix A)	m

symbol	description	unit
Z_0	number of light passes	
α	absorption coefficient	m^{-1}
β	electrolyte efficiency	%
λ	wavelength	m
v	stoichiometric coefficient	
ρ_b	bulk resistivity	Ω.m
ρ_c	specific contact resistance	$\Omega.m^2$
ρ_{met}	resistivity of metal (Copper, Aluminum, etc.)	Ω.m
ρ_{redox}	metal density	$kg.m^{-3}$
τ	minority carrier lifetime	s
ϕ_b	Schottky barrier height	eV
ϕ_m	metal work function	eV
ϕ_s	semiconductor work function	eV
x_s	semiconductor affinity	eV

List of constants

constant	description	value
k_b	Boltzmann's constant	1.3806×10^{-23} J.K^{-1}
q	elementary charge of electrons	1.602×10^{-19} C
C_A	ambipolar Auger coefficient	1.66×10^{-30} cm^6.s^{-1}
n_i	intrinsic carrier density at 300K	9.65×10^{-9} cm^{-3}
F	Faraday's constant	96485 C.mol^{-1}
R_{gas}	universal gas constant	8.3145 J.mol^{-1}.K^{-1}

Table of contents

CHAPTER 1

Introduction

1.1. Thesis motivation

As the title: "Nickel/copper plated contacts as an alternative to silver screen printing for the front side metallization of industrial high efficiency silicon solar cells" indicates, this thesis addresses the field of renewable energy. Burning fossil fuels – oil, coal, and gas – has powered the world economy over the past century and still remain today's dominant source of energy. Apart from the limited resources of fossil fuels and the fact that they often originate from politically unstable regions, their impact on greenhouse gases emissions and the associated risks of climate change force us to develop renewable energies that are economically competitive.

According to the fifth IPCC -Report [IPC13]: "*Carbon dioxide (CO_2) concentrations have increased by 40% since pre-industrial times, primarily from fossil fuel emissions and secondarily from net land use change emissions. Cumulative emissions of CO_2 largely determine global mean surface warming by the late 21st century and beyond. Continued emissions of greenhouse gases will cause further warming and changes in all components of the climate system. Limiting climate change will require substantial and sustained reductions of greenhouse gas emissions*".

Nuclear fission and renewable technologies have a life cycle greenhouse gas emissions that is considerably lower than all other fossil options [WEI07]. Though several countries have active or planned nuclear expansion programs (e.g. France, China, United Kingdom) it remains a questionable source of electricity. Not only uranium resources are limited but the total cost of nuclear electricity generation is debatable as costs - and risks - associated with: i) storing radioactive waste for thousands of years, ii) power-plant decommissioning, and iii) a major nuclear disaster are often not included. Thus, improving energy efficiency and deploying renewable technologies are critical to reduce greenhouse gas emissions and meet the needs of 8.6 billion people with rising living standards that will contribute to the 30% increase in energy demand in the period to 2035 [HOE12]. According to projections by Bloomberg New Energy Finance (BNEF), 70% of the new power capacity built by 2030 will be in the renewable sectors, 75% of which will be in solar and wind sectors [TUR13].

Adding renewable capacities will require massive investments which may be delayed as environmental concerns are appeased by cheap fossil fuels (e.g. shale gas in the USA) and supportive policies for renewable energies weaken because of slow world economy recovery and lower public support. This last point is particularly important in markets with fixed feed-in tariffs (e.g. Germany) where the burden of low – sometimes negative! – wholesale electricity prices and the need to provide back-up capacity because of the intermittent nature of wind and solar power

generation is falling on utilities affecting their profitability. Thus, not only retail electricity prices increase as they include subsidies for renewables but the risks for grid blackouts become higher as utilities put gas-fired power plants, which are no longer profitable, offline [THE13]. Reducing such risks will require new grid infrastructures and regulations in which renewables energies will have to participate for the instability they bring. While achieving electricity prices on par with retail ones (i.e. "grid-parity") was an important milestone for renewable energies such as solar, it is now clear that the actual price per kWh will need to decrease beyond this level.

Solar power generation is largely dominated by photovoltaic (PV) systems which directly convert the incident sun irradiation into electricity. For a PV system, a figure of merit is the levelized cost of electricity (LCOE in €/kWh) which considers its total cost (cost of installation, operation and maintenance, etc.) and the energy generated over its lifetime [BRA11]. The LCOE is impacted by the cost (in €/Wp) of installing a PV system with PV modules and inverters representing about 30% of that cost (installation labor and cables/racking make most of the remaining cost). At present, monocrystalline silicon PV modules costs can be divided in 50% for making the silicon wafer, 20% for the wafer-to-cell costs, and 30% for the cell-to-module costs [VER13]. Reductions in all costs components, particularly in silicon feedstock, have driven PV modules prices down in recent years (see Figure 1.1a). In addition, large capacity expansions (currently >60GW world production capacity for ~30GWp annual market volume) have led to the situation where market prices are below manufacturing costs. While rapidly declining prices are opening new opportunities for PV (e.g. South America), further reductions in manufacturing costs are essential as nearly all PV manufacturers experienced losses in 2012 [CHA13].

As most of a PV system cost is area related, the highest impact on cost can be achieved by increasing the efficiency of the solar cells in the modules while reducing manufacturing costs. This is followed in this thesis by replacing conventional silver (Ag) screen printed front side contacts by nickel/copper (Ni/Cu) plated contacts since they present several advantageous properties including being much cheaper than Ag.

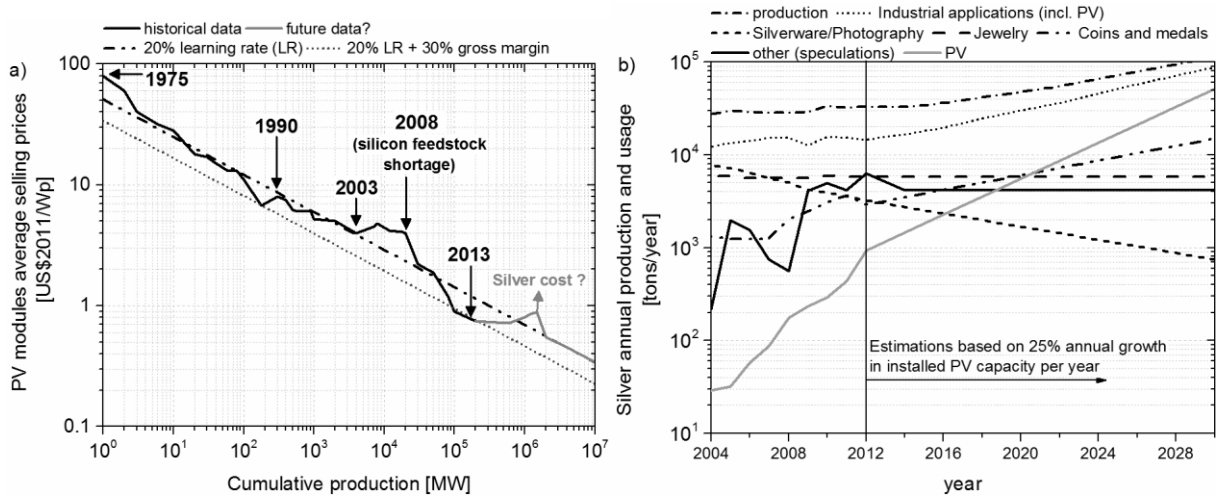


Figure 1.1: a) Photovoltaic (PV) modules learning rate curve (PV modules price versus cumulative production) and speculated impact of Ag. Adapted from [VER13]. B) Silver annual production and usage, adapted from [VER13].

Furthermore, if the installed PV capacity per year continues to grow at the current rate and Ag remains the dominant front side metallization material, within a few years PV will be the major user of Ag (see Figure 1.1b). This will put further pressure on Ag prices which may lead to another supply/cost constrained market after the silicon feedstock shortage around 2008.

1.2. Approach and challenges

The vast majority of industrial silicon solar cells are large area diodes (p-n junction) that are contacted on both sides by metals. A grid-like pattern made up of narrow "fingers" (needed for lateral current transport) and wide "busbars" (needed for integrating cells into modules) is defined at the illuminated front side since complete metal coverage would prevent light from entering the solar cell. Typically, p-type doped silicon substrates are chosen, a shallow n-type ("emitter") region is formed at the front side, and an anti-reflective coating (ARC) is applied at the front side to increase light coupling into the cell. Both front (Ag) and rear (aluminum) contacts are then formed by screen printing and a subsequent high temperature (750–850°C) co-sintering step for a few seconds. However, not only Ag is an expensive material but industrial Ag screen printed contacts also present several limitations (high optical shading, conductivity ~2.5x higher than the conductivity of bulk Ag, poor contact resistance to optimum emitters).

Electrochemical deposition (or plating) of metals is well established for the metallization of semiconductor devices and presents several advantageous properties that make it of interest for the front side metallization of silicon solar cells. In particular, dense metallic layers with high conductivity (close to bulk conductivity) can be selectively plated using relatively cheap and simple electrochemical processes. Given that Cu has a similar conductivity as Ag but is less than a hundredth of the price per kg, Cu-based metallization clearly offers a potential cost advantage. However, a diffusion barrier is required between the silicon substrate and the Cu contacts since diffusion of Cu into the substrate is detrimental to device performance. Thus, the approach followed is to make use of the front ARC as plating mask to define narrow self-aligned Ni/Cu plated contacts where the nickel (Ni) "seed" layer is chosen for its contact and barrier properties.

Despite the potential advantages of Ni/Cu plated contacts (reduced material cost, reduced optical shading, high conductivity, reduced contact resistance to optimum emitters) their commercialization has so far been limited with the notable exception of BP Solar between the years 1992 and 2008. Reasons for this include a number of challenges (increased process complexity, lack of suitable low-cost production techniques/tools at that time, doubts over cost-advantage and long-term reliability) as well as recent progress made with screen printing of Ag. Thus, the approach followed in this thesis is to reduce process complexity by introducing suitable low-cost production techniques/tools in an incremental manner since many processes are inter-linked and need to be co-optimized. Reliability and cost-of-ownership issues are addressed in parallel as it is objective of this thesis to demonstrate a simple/fast/reliable/cost-competitive process to define Ni/Cu plated front contacts in industrial high efficiency silicon solar cells. Alternative cell designs that benefit from the use of Ni/Cu front contacts are also investigated.

1.3. Thesis outline

In **Chapter 2** the *background knowledge* that is needed for this thesis is introduced. This goes from the basic physical principles behind crystalline silicon solar cells to a general description of the processing sequence for making large area two-side contacted silicon solar cells. As this thesis aims at introducing plated front contacts, an emphasis is given on the front side metallization and basic principles of electrochemical deposition of metals are described.

The different *front side metallization technologies* that are currently in production or envisaged for industrial implementation are reviewed in **Chapter 3**. Special attention is drawn to the limitations of industrial Ag screen printed contacts and the resulting pressure to innovate. Technologies enabling the use of Cu as main conductor in a "seed-and-plate" approach are described in greater details. Finally, reasons for choosing self-aligned Ni/Cu plated contacts and challenges to overcome for industrial adoption are presented.

In **Chapter 4** theoretical simulations are performed to evaluate the impact of front emitter design and front metal grid design. Based on these simulations we define *the electrical and design requirements* that should be met by self-aligned Ni/Cu plated front contacts.

As *process simplicity* is key for industrial adoption, efforts made to simplify the front side metallization sequence in high efficiency p-type i-PERC cells are described in **Chapter 5**. After introducing laser ablation of the front anti-reflective coating(s), various methods for depositing the nickel seed layer are thoroughly investigated. A simplified sequence to define Ni/Cu plated front contacts is demonstrated and results obtained when transferring it to industrial pilot-processing plating and sintering tools are presented on industrial size substrates.

In **Chapter 6**, *co-optimization* of standard cell processing steps in p-type i-PERC cells featuring Ni/Cu plated front contacts is discussed based on experimental investigations. A detailed power-loss analysis of the best 12.5x12.5 cm^2 p-type i-PERC device (η=20.5%) fabricated during this thesis is presented in an attempt to direct future efficiency improvements.

The generally observed poor mechanical stability of Ni/Cu plated contacts as compared to conventional screen printed Ag contacts is a great source of concern for industry together with long-term reliability issues associated with the potential risks of Cu or Ni diffusion. Therefore both *reliability issues* are investigated in details in **Chapter 7**.

In **Chapter 8** the simplified sequence to define Ni/Cu plated front contacts is applied to *rear junction n-PERT devices*. Preliminary results obtained with this design are compared to the ones obtained with p-type i-PERC and their respective efficiency potential is discussed.

An alternative technology to form nickel silicides is *excimer laser annealing* which is presented in **Chapter 9**. This technology was applied and optimized for both p-type i-PERC and a novel type of n-type PERT cell based on a heterojunction rear emitter.

In **Chapter 10**, *cost-of-ownership calculations* are performed as the sequence developed in this thesis to define Ni/Cu plated front contacts should not only be simple and reliable but also cost-effective as compared to industrial Ag screen printed contacts.

The main characterization techniques used in this thesis are described in the **Appendix**.

CHAPTER 2

Background knowledge

The present chapter introduces background knowledge needed for the scope of the work in this thesis and has been derived from technical sources. For more detailed information, technical literature is referenced at the beginning of each section. As the vast majority of the work was performed on monocrystalline Si solar cells with a p-doped base and an n-doped front side emitter, the operating principle and loss mechanisms are explained on this type of solar cell (section 2.1). Following this, the fundamentals of metal semi-conductor contacts (section 2.2), electrochemical deposition of metals (section 2.3), crystalline Si solar cell processing and module fabrication (section 2.4) are addressed.

2.1. Crystalline silicon solar cells

Background knowledge presented below was derived from technical literature [GRE86, MCI01, MET07, HOR09, VER12a, BAR12].

2.1.1. Basic physical principles

The ability of silicon solar cells to generate electricity relies on the principles that silicon is a semiconductor and that a solar cell is essentially a large area p-n junction.

In semiconductors and insulators, electrons are confined to a number of energy bands, and forbidden from other regions. The distinction between semiconductor and insulators resides in the magnitude of the energy band gap (E_G) between the lowest occupied band (valence band) and next energy band they may occupy (conduction band). Semiconductors typically have E_G in the 1-4 eV range. In order to excite an electron from the valence band to the conduction band an energy $E \geq E_G$ is required. As the band gap of semiconductors is relatively small, this energy can be provided thermally as well as by absorbing an incident photon. This excitation process results in an "electron-hole pair" as the electron excited to the conduction band leaves behind a hole in the valence band. For indirect band gap semiconductors such as Si (E_G=1.12 eV), the maximum of the valence band and the minimum of the conduction band are positioned at different momentum (Figure 2.1a). If the photon energy is of the same order as the band gap width, excess momentum has to be transferred to or from lattice vibrations (phonons), to make excitation possible. Requiring phonons means that the probability of the electron-photon interaction lowers, which decreases the absorption coefficient greatly. This requires efficient light trapping schemes for long wavelength photons (see section 2.3). As a result of phonon interaction, transition from absorption to non-absorption is not sharp and photons with energy slightly lower than E_G,

corresponding to wavelengths slightly above 1100 nm, have still a (small) probability to be absorbed. Excited carriers remain in this state for some time ("lifetime", τ) and randomly move a certain distance (diffusion length) until they recombine (see section 2.1.3 for recombination mechanisms) unless they can be collected before that.

For silicon solar cells, a p-n junction is formed by overcompensating the base doping with opposite doping. At the metallurgical junction between both doped regions, free electrons from the n-type region (typically phosphorous doped) recombine by diffusion with a hole in the p-type region (typically boron doped) due to concentration differences. This leaves behind a positively charged (ionized) phosphorous atom in the n-type region and a negatively charged (ionized) boron atom in the p-type region. The charge due to the ionized dopant atoms creates an electric field resulting in a drift current in the opposite direction to the diffusion current. Equilibrium is reached when both drift and diffusion currents have the same magnitude. The ionized dopant atoms remain in the area which is depleted of free charged carriers forming the "space charge region" (SCR) or depletion region (Figure 2.1b). In industrial solar cells, the p-n junction is typically formed by a thin 0.2 to 2 µm n-doped layer ("emitter") located at the irradiated side and a thick 50 to 200 µm p-type substrate. Electrons-holes pairs are generated under illumination. Minority carriers (electrons in p-type substrate, holes in n-type emitter) diffuse randomly to the p-n junction where they are separated by the electric field and become majority carriers. This greatly reduces recombination probability and the current flow can be extracted at the front and rear side contacts by an external bias.

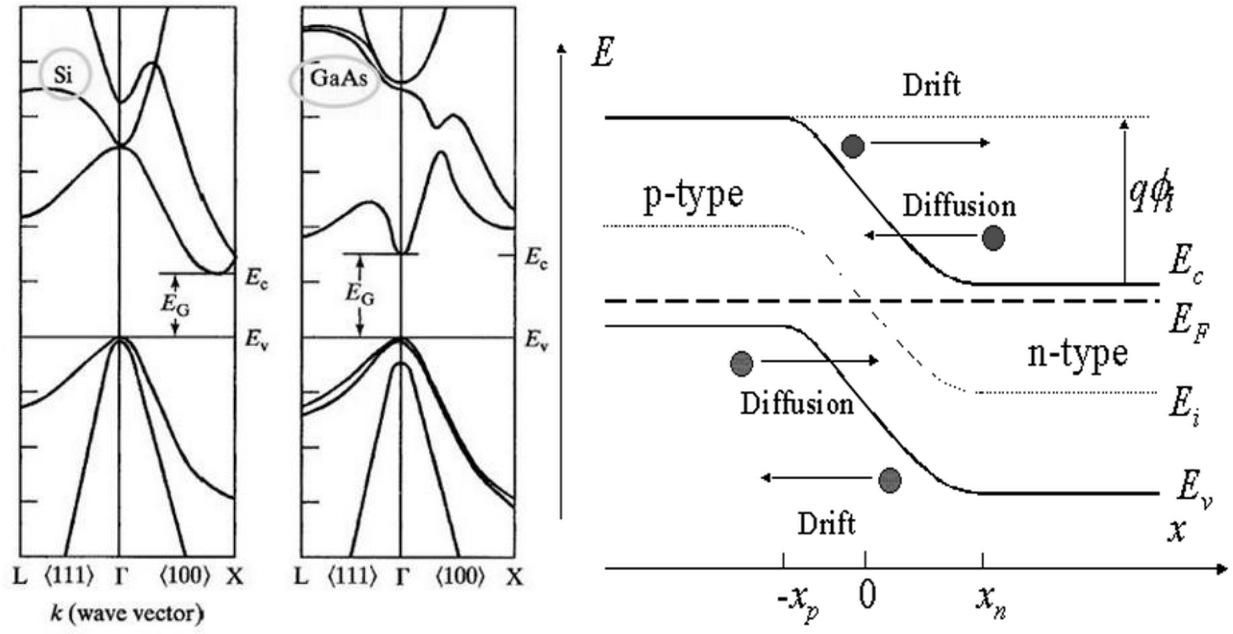


Figure 2.1 a) Energy band diagram of an indirect (Si) and direct (GaAs) semiconductor. Energy is plotted as a function of wave vector (k) since the band diagram depends on the direction in the crystal lattice. b) Energy band diagram of a p-n junction at thermal equilibrium.

2.1.2. Current-voltage curves

Typical industrial silicon solar cells are large area diodes (p-n junction) with a shallow emitter and a thick base which can simply be described by the one diode model [MET07]:

$$j(V) = j_0 \left(\exp\left(\frac{q \cdot V}{k_b \cdot T}\right) - 1 \right) - j_{ph} \quad (2.1)$$

with q being the elementary charge, k_b the Boltzmann's constant, T the temperature, j_0 the dark saturation current density w, and j_{ph} the photo-generated current density.

As indicated by this equation, the photo-generated current flows in the opposite direction to the forward biased (dark) diode shifting the illuminated current-voltage (I-V) characteristic to negative values as shown in Figure 2.2.

Cell parameters can be obtained from the measured illuminated I-V curve of a solar cell. Illuminated I-V measurements are usually performed under standard test conditions (STC: T=25˚C, light intensity 1000 W/m^2, spectral distribution AM1.5g). From this measurement, the cell power density P which is the product of current density and voltage can be obtained as shown in Figure 2.2. The cell power density has its maximum defined as P_{mpp}. The current density and the voltage at this point are called j_{mpp} and V_{mpp} respectively. The open-circuit voltage V_{oc} and the short-circuit density j_{sc} are obtained from the intersection points of the I-V curve with the voltage and current axis respectively. From these parameters, the energy conversion efficiency ŋ of a solar cell, which describes the ratio of the maximum power produced by the solar cell (P_{mpp}) to power of incident light (P_{in}), is defined by the following equations:

$$ŋ = \frac{P_{mpp}}{P_{in}} = \frac{j_{mpp} \cdot V_{mpp}}{P_{in}} = \frac{j_{sc} \cdot V_{oc} \cdot FF}{P_{in}} \quad (2.2)$$

with FF being the fill factor which is described in equation (2.3). The fill factor can be regarded as the ratio of two squares: the largest fitting square under to I-V curve to the square defined by the product of V_{oc} and j_{sc}.

$$FF = \frac{j_{mpp} \cdot V_{mpp}}{j_{sc} \cdot V_{oc}} \quad (2.3)$$

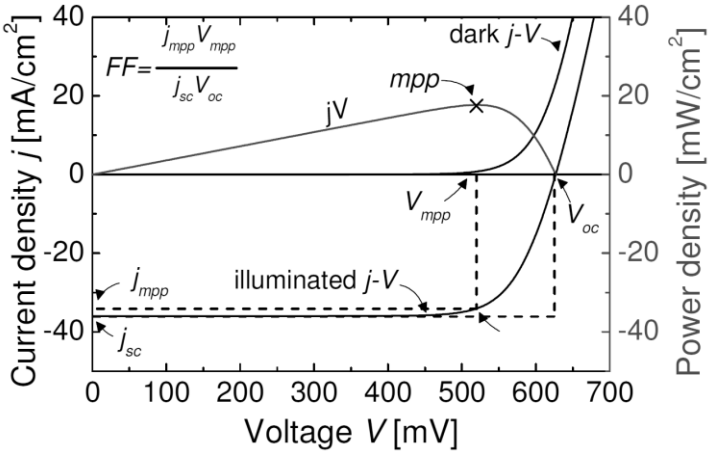


Figure 2.2 Illuminated I-V, power density, and dark I-V curves versus voltage of the solar cell [MET07].

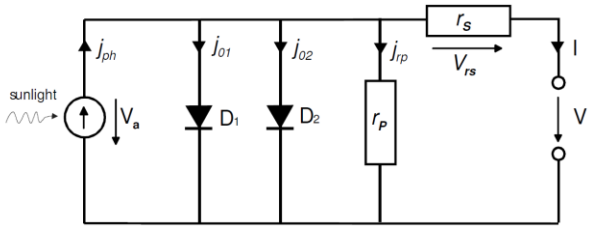


Figure 2.3 Equivalent circuit diagram of a solar cell based on two-diode model [MET07].

The one-diode-model can be extended to take into considerations the impact of series resistance r_s, parallel resistance r_p (or shunt), and recombination in the space charge region (SCR). The second diode connected in parallel models the recombination in the SCR under the assumption of a single mid-gap recombination center with a constant recombination rate across the SCR. The two-diode equation is given as follows:

$$j(V) = j_{01}\left(\exp\left(\frac{q\cdot(V-|j\cdot r_s|)}{n_1.k_b\cdot T}\right)-1\right)+j_{02}\left(\exp\left(\frac{q\cdot(V-|j\cdot r_s|)}{n_2.k_b\cdot T}\right)-1\right)+\frac{V-|j\cdot r_s|}{r_p}-j_{ph} \qquad (2.4)$$

where j_{01} represents the recombination current density in the emitter and base regions and j_{02} the recombination current density in the space charge region. The factors n_1 and n_2, which are called the ideality factors, describe the quality of the single diodes and should be n_1=1 and n_2=2.

The cell parameters j_{01}, j_{02}, r_s, and r_p can be extracted by performing a dark I-V measurement (j_{ph}=0) and fitting the curve according to equation (2.4) as shown in Figure 2.4. For each component of the dark I-V curve, the local ideality factor m can be derived from [MCI01]:

$$m(V) = \frac{k_b\cdot T}{q}\left[\frac{d(V-|j\cdot r_s|)}{d(\ln j)}\right] \qquad (2.5)$$

For the front side metallization, r_s, r_p, and j_{02} are of particular interest as they are affected by the contact formation. However, the contribution of the emitter to r_s is reduced in the dark thus dark I-V fitting is not the best way to determine r_s [PYS07]. Also, fitting dark I-V characteristics according to equation (2.4) might not be possible as many effects (e.g. scratches, higher recombination in the SCR under the front contacts) can cause a local increase in recombination leading to a "hump" at mid-voltage values in both the dark I-V and m-V curves.

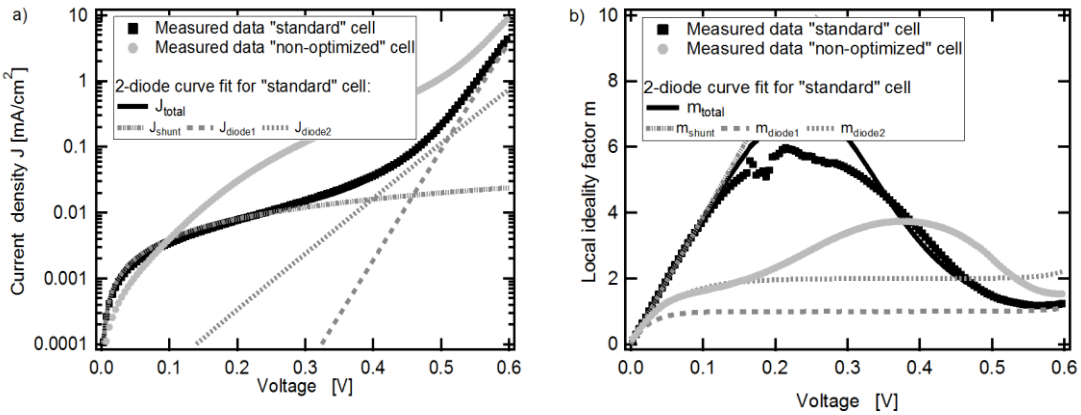


Figure 2.4 Measured dark I-V (a) and local m-V curves (b) for a "standard" solar cell behaving closely to the two-diode model and a "non-optimized" solar cell suffering from higher j_{02} recombination under the front contacts.

2.1.3. Loss mechanisms

General losses

Single junction Si solar cells are theoretically limited to energy conversion efficiencies of about 29% at 1 sun [SWA05]. This is mostly driven by the inability of Si solar cells to fully exploit the AM1.5g solar spectrum as shown in Figure 2.5. Long wavelengths photons thus with an energy $E < E_G$ (E_G=1.12 eV for Si) cannot generate electron-hole pairs while a high energy photon ($E >> E_G$) will only create one electron-hole pair (excess energy is lost in heat).

The maximum achievable open-circuit voltage ($V_{oc,max}$) is not limited by the band gap but by the separation of the quasi-Fermi levels which are defined by base and emitter doping levels. Auger recombination further limits $V_{oc,max}$ which can be estimated from the following equation where the maximum short circuit density $j_{sc,max}$ is obtained by integration of the AM1.5g spectrum assuming Lambertian limit for the rear reflectance and a wafer thickness W=160 µm:

$$V_{oc,max} = \frac{n \cdot k_b \cdot T}{q} ln\left(\frac{j_{sc,max}}{q \cdot C_A \cdot n_i^3}\right) \quad (2.6)$$

where q is the electron charge, n the ideality factor (n=2/3 when limited by Auger recombination), k_b the Boltzmann constant, and T the absolute temperature.

With an ambipolar Auger coefficient C_A=1.66x10^{-30} cm^6/s, n=2/3, the intrinsic carrier density n_i=9.65x10^{-9} cm^{-3} (at T=300 K) [WOL10] and $j_{sc,max}$= 44.01 mA/cm^2 equation (2.6) gives a maximum $V_{oc,max}$~756 mV. In practice, V_{oc} values up to 750 mV have been reported [YAN13].

The maximum fill factor is not defined by the product of open-circuit voltage and the short circuit density (FF=100%) as the current depends exponentially on voltage. This limits the maximum achievable fill factor which can be estimated from an empirical relation [GRE81]:

$$FF_0 = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \quad (2.7)$$

with the normalized voltage $v_{oc} = q \cdot V_{oc}/(n \cdot k_b \cdot T)$ (2.8)

Equation (2.7) gives a maximum fill factor ~89% when limited by Auger recombination (n=2/3). In practice, n values are found close to 1 and maximum fill factor are limited to ~85% [SWA05].

Optical losses, recombination losses, and electrical losses further limit the achievable efficiencies. The highest measured value for a Si solar cell under standard conditions is 25% for a small area device [ZHA99] and 24.7% for a large area (100 cm^2) device [YAN13].

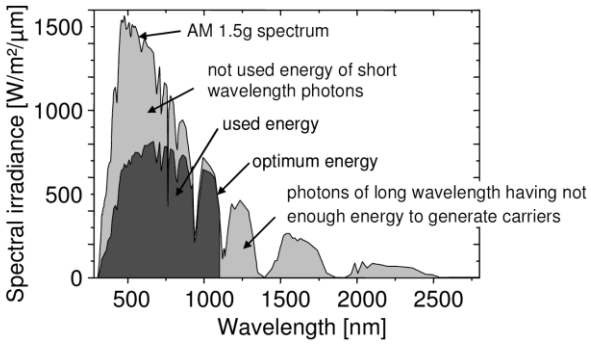


Figure 2.5 AM1.5g spectrum vs. wavelength, the dark area shows the irradiance used by a Si solar cell [MET07].

Optical losses

Optical losses are caused by reflection at the front surface, free carrier absorption, and transmission outside silicon. In two side contacted solar cells, reflection at the front surface is caused by reflection at the front side contacts and at the un-metallized regions. Reducing reflection at the front side contacts results in a trade-off between j_{sc} losses and series resistance losses (see Chapter 4.2). Reflection at the un-metallized regions can be lowered by applying a front side texture reducing reflectivity at the front side from about 30% (flat Si) to about 10% (random pyramid textured Si). Applying an anti-reflection layer, which also serves as passivation layer to reduce recombination at the surface, further reduces the reflectivity to about 5%. Free carrier absorption (FCA) occurs when a carrier is excited from a filled state to an unoccupied state in the same band. Free carrier absorption increases linearly with doping and to the square with wavelength and hence can become an important parameters at long wavelengths [SCH78]. It results again in a trade-off as reducing doping, particularly in the front emitter for conventional cells, to reduce FCA results in increased series resistance losses. Transmission losses are occurring at the front and rear side. Since Si is an indirect semiconductor, its absorption coefficient is low which means that long wavelengths photons can travel a long distance (several times the wafer thickness) before generating electron hole pairs. To reduce transmission losses, the incident light needs to be efficiently coupled or "trapped" in Si so that long wavelengths photons are reflected multiple times at the front and rear side. In two side contacted solar cells, this is achieved by using a highly reflective metal layer (typically aluminum), which also serves as rear contact, to improve internal rear reflectance. In more advanced solar cell concepts, light-trapping is further enhanced by using dielectric layers between Si and the rear metal contact.

Recombination losses

Light generated carriers randomly move a certain distance (diffusion length) until the time they recombine ("lifetime", τ) unless they reach the p-n junction which increases their collection probability dramatically (see section 2.1.1). There are four different recombination mechanisms: a) radiative recombination, b) Auger recombination, b) recombination via recombination centers in the bulk (Shockley-Read-Hall), and d) recombination via surface states. All four mechanisms are represented in Figure 2.6 and will be briefly described in this section.

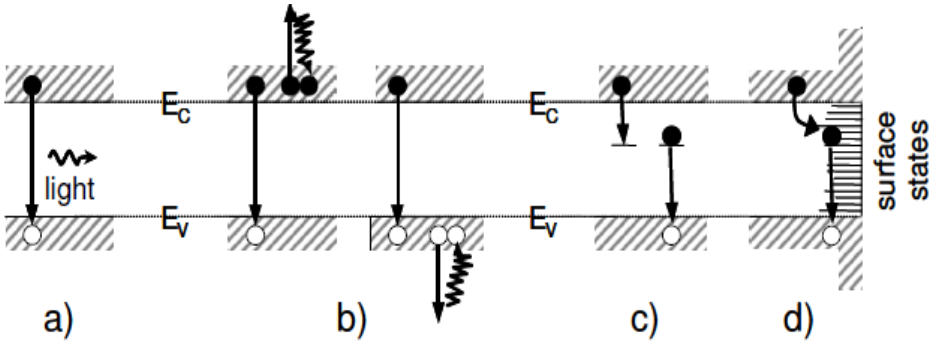


Figure 2.6 Recombination mechanisms in silicon solar cells: a) radiative recombination, b) Auger recombination, c) recombination via recombination centers in the bulk, and d) recombination via surface states [MET07].

Radiative recombination is the inverse process of optical absorption. It involves a conduction band electron falling from an conduction band state into a vacant valence band state and releasing its energy as a photon (see Figure 2.6a). For indirect band gap semiconductors such as Si, radiative recombination involves the participation of a phonon to maintain momentum and hence it is considered to be negligible compared to other recombination processes.

Auger recombination is regarded as a three-particle interaction. It involves a conduction band electron recombining with a vacant hole in the valence band with the excess energy being transferred to third particle (electron or hole) in the conduction band. The excited electron or hole quickly thermalized back to the band edge by losing its energy in form of phonons as shown in Figure 2.6b. Auger recombination becomes the dominant mechanism at high injection levels (large amount of excess carriers) and is increased with increased doping levels. In reality, Auger recombination is more complicated and general parameterizations have been proposed based on experimental observations of Auger recombination in Si [RIC12].

Recombination via recombination centers in the bulk was first described analytically by Shockley-Read-Hall [SCH52, HAL52] and hence is also named SRH recombination. It involves the presence of discrete energy levels within the band gap which are created by impurities, particularly metals like Fe or Cu, or by crystallographic imperfections (point defects, dislocations). These energy levels greatly facilitate recombination via a two-step process whereby an electron from the conduction band first relaxes to the defect energy level and then relaxes to the valence band where it recombines with a vacant hole (Figure 2.6c). SRH recombination is important in Si solar cells as defects can originate from crystal growth or un-desired contamination. On the other hand, their impact can be reduced by gettering (forming clusters of impurities) or by passivating trap levels (e.g. H release from silicon nitride anti-reflective coating upon high temperature contact sintering).

Recombination via surface states results from the fact that the crystal lattice abruptly ends at the surface (dangling bonds) giving rise to a high density of defect states. Even if the surface of Si is not bare, say due to silicon nitride anti-reflection coating, the presence of silicon-nitride bonds can stress the crystal structure at the surface which again introduces many defect states. Recombination at the surface can be described using an extended SRH model [VER12a]. Fundamentally, reduction of surface recombination can be achieved by i) reducing the density of interface traps (D_{it}) and ii) minimizing the concentration of minority carriers at the surface. In practice, a reduction of D_{it} can be obtained by using an appropriate dielectric layer such as silicon oxide, silicon nitride, or aluminum oxide to passivate dangling bonds. Minimizing the concentration of minority carriers at the surface can be achieved by doping (e.g. back surface field, see section 2.3.2) or by using dielectric layers with fixed charges (e.g. aluminum oxide on a p-doped surface, see section 2.3.2) creating an electric field to repel minority carriers.

Electrical losses

Real solar cells are better described using a two-diode model which takes take into considerations electrical losses caused by series resistance r_s and shunt resistance r_p. Both have a strong impact on the maximum point whereas the V_{oc} or the j_{sc} values are only affected for very high r_s or low r_p values as shown in Figure 2.7. The parallel resistance describes the possibility of separated carriers to recombine via parasitic currents between the n and p-type regions. The series resistance describes the resistance of all individual sections of the cells photo-generated carriers have to pass through before they reach the external load and hence are different at cell level and at module level (see section 4.2). Series resistance at cell level can be extracted by different ways with r_s extraction from 2 light-level measurements giving good results [PYS07].

A good method to quantify the impact of series resistance losses is to extract the pseudo fill factor (pFF) from Suns-Voc measurements [SIN00, BOW01]. As the pFF is determined without any current flowing it is free of series resistance losses. Comparing the pFF to the measured fill factor (FF), the FF losses due to series resistance losses can be extracted. The difference between the ideal FF_0 given in equation (2.7) and the pFF allows to quantify FF losses due to recombination in the space charge region (j_{02}) and to linear shunts (r_p) which can be caused by front side metallization but also by other processes [MCI01]. Such a comparison of the different FFs is shown in table 2.1 and the measured absolute FF losses are given in Figure 2.8.

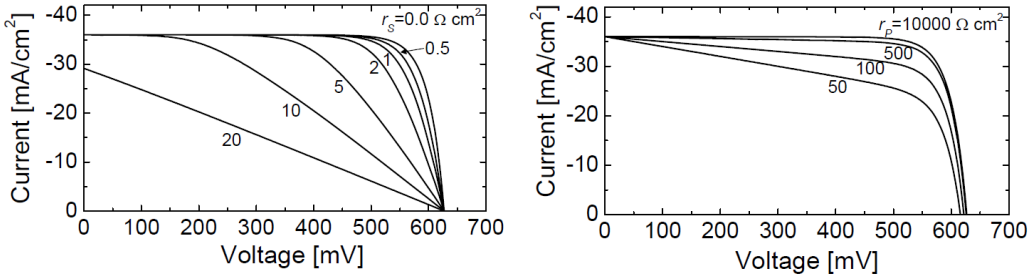


Figure 2.7 Effect of series resistance (left-hand) and parallel resistance (right-hand) on I-V characteristics [MET07].

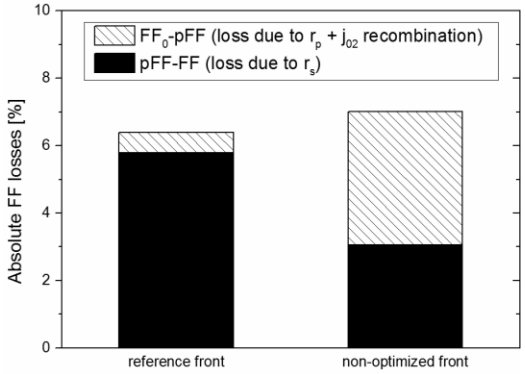


Figure 2.8: Absolute FF losses due to series resistance r_s (pFF-FF) or to recombination in the space charge region and liner shunts (FF_0-pFF) for a reference front side metallization and a non-optimized front side. For the cell with non-optimized front side, performing an additional dark I-V measurement allowed to attribute the absolute FF loss to a local increase in j_{02} recombination under the front contacts (see Figure 2.4)

Table 2.1: Fill factors for two different types of solar cells. j_{sc}, V_{oc}, FF, ŋ values are obtained from illuminated I-V measurement. The pseudo FF (pFF) is measured using Suns-V_{oc}. The ideal FF_0 is calculated from V_{oc} according to equation (2.1.3). r_s is determined from 2 light level I-V measurements.

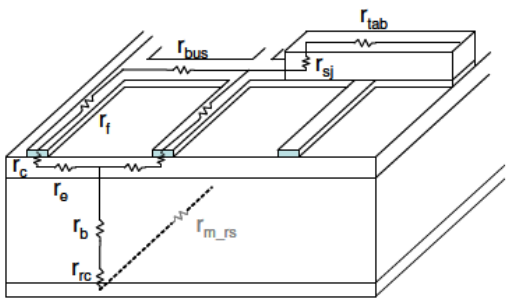
name	j_{sc}	V_{oc}	FF	ŋ	pFF	FF_0	r_s
	[mA/cm^2]	[mV]	[%]	[%]	[%]	[%]	[Ohm.cm^2]
reference front metallization	38.1	651.0	77.3	19.2	83.1	83.7	1.1
non optimized front metallization	37.7	642.0	76.5	18.5	79.5	83.5	0.6

Loss mechanisms due to front side pattern

As the front side metallization is at the irradiated side, optical losses caused by reflection at the front metal grid and electrical losses need to be balanced. For large-area industrial silicon solar cells this is typically achieved using an H-pattern for the front grid (see section 2.4.1) with narrow fingers transporting the current to busbars where cell-to-cell interconnections are made at module level using metal tabs (see section 2.4.3). The total series resistance is the sum of all individual series resistance contributions as shown in Figure 2.9.

The finger resistance, front contact resistance, and emitter resistance are of primary importance in this work. Reducing the width of the front fingers to minimize grid shading leads to increased finger resistance and also reduces the contact area with the emitter which may lead to increased contact resistance values depending on the specific contact resistance value (see section 2.2). Using lowly doped emitters reduces Auger recombination, SRH recombination, and reduces free carrier absorption. However, it also leads to increased lateral resistance and may lead to i) increased contact resistance, ii) increased recombination under front contacts, iii) increased recombination in the space charge region (j_{02}), and iv) increased risks of shunts (r_p).

Large-area industrial silicon solar cells may also suffer from strong non-uniformities. Such non-uniformities may result in characteristic “humps” in the m-V curve leading to ideality factors well above 1 at voltage values close to V_{mpp} , and hence can strongly reduce the fill factor and the V_{oc}. An example of such a hump in the m-V curve was shown in Figure 2.4.



r_{m_rs}: resistance of rear side metal layer
r_{rc}: contact resistance of rear side to base
r_b: resistance of base
r_e: resistance of emitter
r_c: contact resistance of front grid to emitter
r_f: line resistance of finger
r_{bus}: line resistance of busbar
r_{sj}: contact resistance of soldering joint
r_{tab}: line resistance of tab
r_{ext}: line resistance tab extension

Figure 2.9: Cross-section schematic of a solar cell showing the different series resistance contributions [MET07].

2.2. Metal-semiconductor contact

Background knowledge on metal semiconductor contacts presented in this section is derived from technical literature [SCH84, MET07, HOR09a, STA09, THI13].

The ideal contact for a solar cell should be as small as possible, oppose negligible resistance to current transport, and should not degrade device performance. The first metal-semiconductor contacts had a rectifying behavior meaning that the current could flow easily only in one direction. The first generally accepted theory was described by Schottky who introduced the notion of potential barrier forming at the metal-semiconductor interface [SCH39]. In the Schottky model, when a metal and a semiconductor are brought into intimate contact their Fermi levels need to equalize via charge transfer and this results in bending of the energy band diagram as shown in Figure 2.10 for n-type Si. The formed Schottky barrier ($\emptyset_b$) can be described as the difference between the metal work function ($\emptyset_m$) and the semiconductor affinity (X_s) with the resulting potential difference across this region (built-in voltage: V_{bi}) simply being the difference between $\emptyset_m$and the semiconductor work function ($\emptyset_s$). This gives for n-type semiconductors:

$$q\emptyset_b = q\emptyset_m - qX_x \quad (2.9)$$

and

$$qV_{bi} = q\emptyset_m - q\emptyset_s \quad (2.10)$$

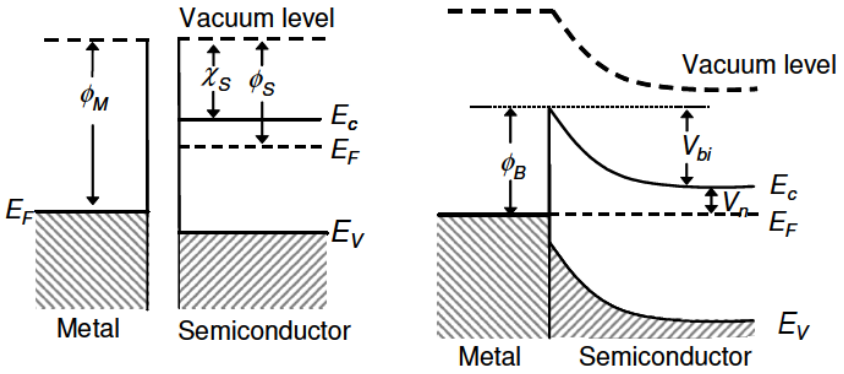


Figure 2.10: Energy band diagram of a metal- n-type semiconductor contact before and after bringing them into contact. The formed Schottky barrier $\emptyset_b$ can be described as the difference between the metal work function $\emptyset_m$and the semiconductor affinity (X_s). [MET07].

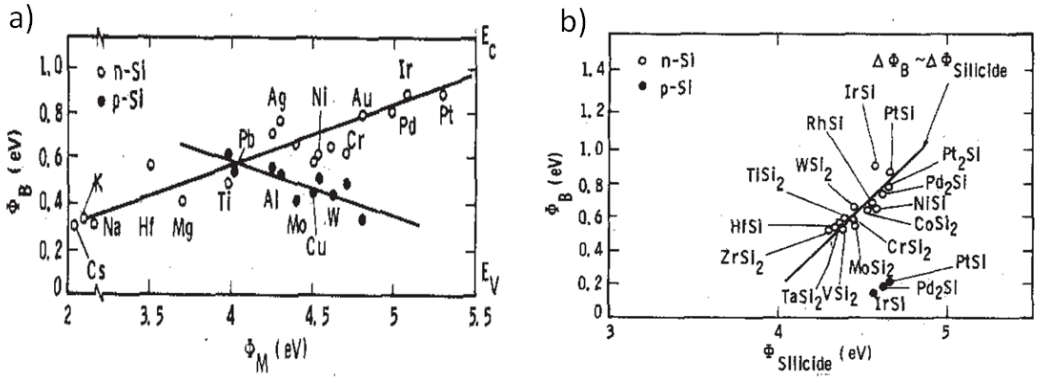


Figure 2.11: a) Measured barrier height $\emptyset_b$ versus metal work function $\emptyset_m$ for (a) metal to n- and p-type silicon and (b) silicide to n- and p-type silicon [SCH84].

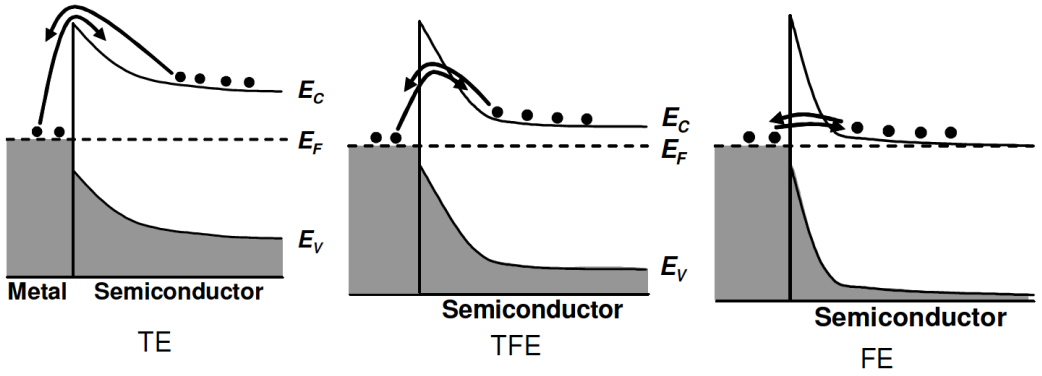


Figure 2.12: Current flow mechanisms between metal and semiconductor. From left to right: thermionic emission (TE), ii) field emission (FE), and iii) thermionic field emission which is combination of TE and FE [MET07].

For metals, the relationship between the potential barrier $\emptyset_b$ and the metal work function $\emptyset_m$ is weaker (slope ~0.3) than predicted by the Schottky model (see Figure 2.11a). The influence of surface defect states was proposed as extension to the Schottky theory to explain this [SCH84]. For silicides (see Figure 2.11b), the behavior is approaching the one predicted by the Schottky model (slope ~1) which is likely due to surface defect states playing a less important role since the silicide-Si interface is within silicon (silicide formation consumes Si).

Transfer of charges from metal to semiconductor can be described by three mechanisms: i) thermionic emission (TE), ii) field emission (FE), and iii) thermionic field emission (i.e. combination of TE and FE, see Figure 2.12). Thermionic emission, which is caused by thermal activation over the barrier, is dominant up to doping concentration around $1x10^{17}$ cm^{-3}. For higher doping concentrations, the width of the space charge region at the metal-semiconductor interface is narrowing and the probability for quantum tunneling becomes significant. Field emission becomes the dominant mechanism for doping concentrations above $1x10^{20}$ cm^{-3}.

A figure of merit for ohmic contacts is the specific contact resistance ρ_c expressed in $\Omega \cdot cm^2$. The theoretical definition of ρ_c is the reciprocal of the derivative of current density (j) with respect to the voltage (V) at zero bias [SCH84]:

$$\rho_c = \left(\frac{\partial j}{\partial V}\right)^{-1}_{V=0} \qquad (2.11)$$

To facilitate calculations, we used the specific contact resistance ρ_c unified in one equation as described in [THI13] for n-type Si. Specific contact resistance results plotted for different barrier height $\emptyset_b$ are given in Figure 2.13a and compared to literature data extracted for nickel silicide (NiSi) using advanced contact resistance test structures (see appendix A). A good agreement is obtained for $\emptyset_b$ =0.6 eV. To better understand the importance of ρ_c, its impact on efficiency was computed as a function of contact opening. From the results given in Figure 2.13b, it becomes clear that reducing the contact opening width (width of metal in direct contact with Si) increases efficiency as shading losses are reduced. However, the optimum contact opening width strongly depends on the ρ_c and hence it is desired to achieve ρ_c<$1x10^{-3}$ $\Omega.cm^2$. Going back to Figure 2.13a, metals (or alloys) with low barrier height and high surface doping are preferred to achieve ρ_c < $1x10^{-3}$ $\Omega.cm^2$.

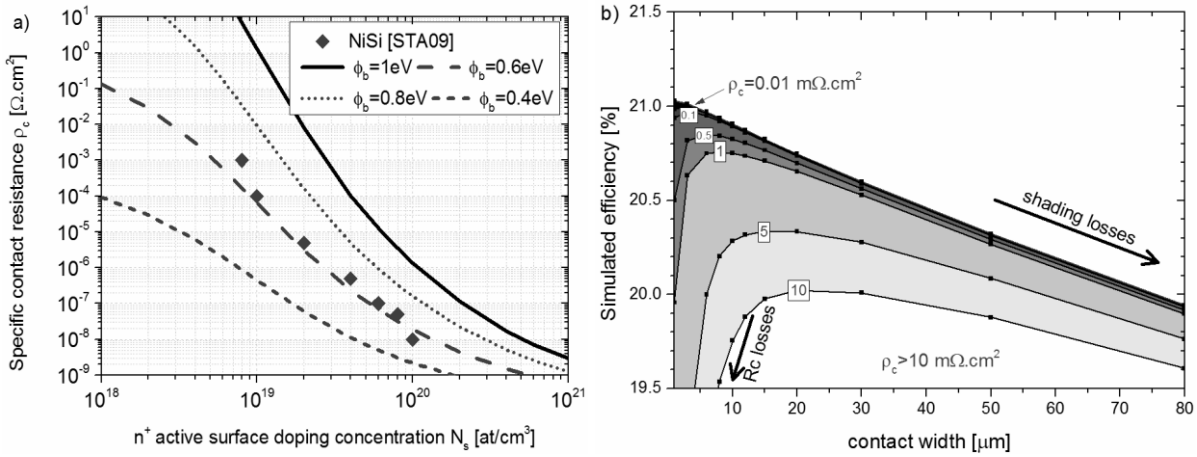


Figure 2.13: a) Specific contact resistance ρ_c on n^+-doped p-type Si(100) for different barrier heights values versus active surface dopant concentration N_s computed using a unified equation for ρc [THI13]. Measured ρ_c values for nickel silicide on n-type Si(100) are given in [STA09]. b) Simulated solar cell efficiency for different ρ_c values as a function of contact opening width. Detailed calculations are given in Chapter 4.

2.3. Electrochemical deposition of metals

In this section, basic principles of electrochemical deposition of metals are described together with terminology used in this thesis. Information presented here and further details beyond that can be found in technical literature [BAR01, BAR12].

Electrochemical deposition of metals involves the transfer of electrons between electrodes (metal or semiconductor where charge is transported via electrons and holes) and an electrolyte containing the metal ions. Metal ions within the electrolyte can be oxidized (requires the loss of an electron) or reduced (i.e. acceptance of an electron) giving a "Redox-couple":

$$v_O O^{z+} + ze^- \leftrightarrow v_R Red \tag{2.12}$$

where z is number of electrons transferred during the reaction, O is the oxidized metal species and Red is the reduced metal species, with their stoichiometric coefficient v.

The electrochemical potential E_{redox} is given by Nernst's equation:

$$E_{redox} = E_0 + \frac{R_{gas} \cdot T}{z\,F} ln\left[\frac{C_O}{C_R}\right] \tag{2.13}$$

where E_0 is the standard potential of the Redox-couple, F is the Faraday constant (F=96485.34 C.mol^{-1}), R_{gas} the universal gas constant (8.3145 J.mol^{-1}.K^{-1}), T the temperature. C_O, C_R, represent the concentrations (roughly activities) of the oxidized and reduced species respectively.

Both potentials E_{redox} and E_0 are given versus a reference. Typically, the "normal hydrogen electrode" (NHE) is used as reference point. The standard potential E_0 of the NHE is 0V and other used reference electrodes are tabulated in literature against NHE [COM96].

The quantity of reduced (or oxidized) species is related to the number of electrons transferred via Faraday's law:

$$Q = n \cdot z \cdot F \tag{2.14}$$

where Q is the charge, n the amount of reduced (or oxidized species) in mol, and z the number of electrons required for the reaction of one species.

In the case of metals, the deposited mass m is related to the charge via the molar mass M and the electrolyte efficiency β according to Faraday's second law:

$$m = \beta \frac{M \cdot Q}{z \cdot F} \tag{2.15}$$

To run an electrochemical process, a polarization is necessary at one electrode (called working electrode). However, this is not possible without an oppositely polarized process at a counter electrode. The electrode at which the reduction processes take place is called anode while the electrode at which oxidation processes take place is called the cathode. Electrochemical systems that run spontaneously are called galvanic cells. Galvanic cells (e.g. discharging battery) deliver a current and a voltage between the cathode (positively charged) and the anode (negatively charged). On the other hand, a system where a voltage and a current are applied externally to force a positive polarization of the anode is called an electrolytic cell.

The number of charges transferred can be related to the current I passing through the cathode during a duration t (i.e. plating time) via the following equation:

$$Q = I \cdot t \tag{2.16}$$

Using equation (2.15) and (2.16), the theoretical thickness of metal plated at the cathode over an area A_{metal} can be calculated by:

$$h = \frac{m}{\rho_{metal} \cdot A_{metal}} = \beta \frac{M \cdot I \cdot t}{\rho_{metal} \cdot A_{metal} \cdot z \cdot F} = \beta \frac{M \cdot j \cdot t}{\rho_{metal} \cdot z \cdot F} \tag{2.17}$$

where ρ_{metal} is the metal density in g/cm^3 and j the plating current density in A/cm^2.

The interface between the electrode and the electrolyte is of particular interest since electrochemical processes occur there. Electrode-electrolyte interfaces are generally described by an electrochemical double layer as shown in Figure 2.14. Ions (positively or negatively charged) that are adsorbed at the electrode surface due to chemical interactions and may inhibit charge transfer define the so-called "inner Helmholtz plane" (IHP). Solvated or complexed ions that are inversely polarized to the electrode may diffuse to it, under the influence of Coulomb force and thermal motion, only as far as their coordination sphere allows thereby defining the so-called "outer Helmholtz plane" (OHP).

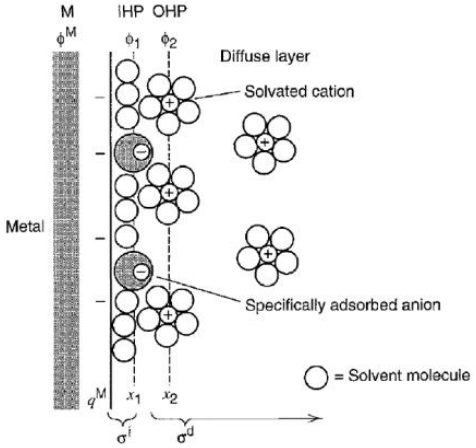


Figure 2.14: Electrode-electrolyte interface schematically represented by an electrochemical double layer. M: Metal, IHP: Inner Helmholtz plane, OHP: Outer Helmholtz plane. [BAR01]

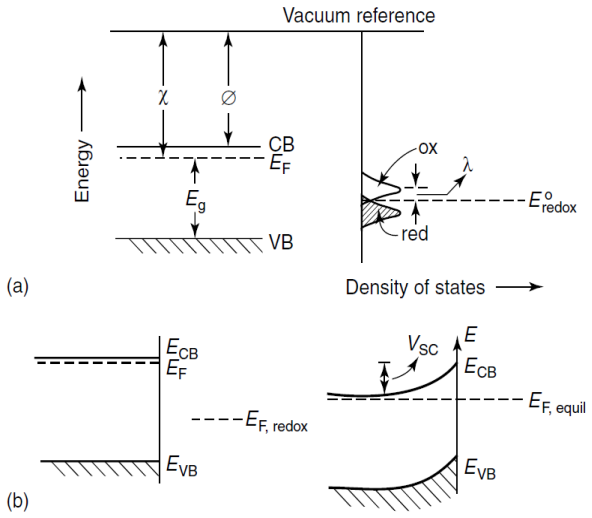


Figure 2.15: (a) Energy levels in a semiconductor (left-hand) and in a redox electrolyte (right-hand) shown against the vacuum level. X and Φ are the semiconductor electron affinity and work function, respectively. (b) Semiconductor-electrolyte interface before (left-hand) and after (right-hand) contact for a n-type semiconductor [BAR01].

Table 2.2: Selected redox potential versus a "normal hydrogen electrode" (NHE), versus a "saturated calomel electrode" (SCE= +0.24 V vs. NHE), versus the vacuum level, and towards n-type silicon (approximated).

Redox-couple	E_0 [V vs. NHE]	E_0 [V vs. SCE]	$\emptyset$ [eV]	ΔE to n-type silicon (10^{20} cm-3) [eV]
$Ni^{2+}+2e^- \leftrightarrow Ni$	-0.23	-0.47	-4.27	-0.22
$Cu^{2+}+2e^- \leftrightarrow Cu$	+0.35	+0.11	-4.85	-0.8
$Ag^{+}+e^- \leftrightarrow Ag$	+0.8	+0.56	-5.3	-1.25

For electrochemical deposition of metal on semiconductor it is important to consider the semiconductor-electrolyte interface. Upon immersing a semiconductor in a redox electrolyte, the electrochemical potentials (Fermi levels) need to equalize leading to "band bending" in the semiconductor. While estimates vary [BAR01], the "saturated calomel electrode" (SCE) potential appears to lie at -4.5 eV versus the vacuum level and hence the electrochemical potentials of the semiconductor-electrolyte can be compared in a band diagram as shown in Figure 2.15. For a n-type semiconductor (which will be always the case in this thesis), the Fermi level (-4.05 eV) is typically higher than the redox potential of the electrolyte (see Table 2.2) and hence electrons will be transferred to the electrolyte. This results in a upward band bending, as shown in Figure 2.15b, which is also called overpotential. Unlike with metal-electrolyte interface where almost all the potential drop is within the electrolyte double layer, the potential drop is partitioned between the overpotential and the double layer. Thus, besides its behavior as resistor (resistance to current transport), the Si-electrolyte also shows double capacitance effects.

As for metallic electrodes, applying an external potential shifts the Fermi levels and hence the magnitude and direction of band bending at the semiconductor-electrolyte interface vary with the applied potential. At a certain applied potential, called flat-band potential (E_{FB}), the

Fermi levels of the semiconductor and the electrolyte are equal (no transfer of charge, no band bending). For an n-type semiconductor, accumulation (excess electrons at interface) is obtained at potentials negative of this flat-band potential ($E < E_{FB}$) while depletion (upward band bending) is obtained at potentials positive of the flat-band voltage ($E > E_{FB}$).

The application of light to a semiconductor-electrolyte can influence the charge carrier potential at the interface In the case of n-type semiconductor and for $E > E_{FB}$ an inversion layer exists. Photo-generated carriers can be separated by the space charge region and holes move toward the interface extracting an electron form a solution species. In that case, the n-type semiconductor acts as a photo-anode (i.e. oxidation). Similarly, solar cells (p-n junction) feature an additional space charge region in the bulk which can separate photo-generated carriers leading to an increase of electrons at the n-type surface (i.e. accumulation at n-type surface).

The behavior discussed above applies to idealized semiconductor-electrolyte interfaces. As with the metal-semiconductor contacts, interface defects causing energy states in the band gap can strongly affect the behavior of semiconductor-electrolyte interfaces. Oxidation of silicon by holes in the depletion region can also prevent metal reduction.

2.4. Crystalline Si solar cell processing and module fabrication

*In this section, standard large area silicon solar cell processing and advanced cell structures which are envisaged for industrial implementation or which are currently in use for high-end applications are introduced. Further details beyond that can be found in journal papers published in 2007 [GLU07, NEU07], in 2012 [ABE12], and in 2013 [*MET13*]. The different technologies used for front side metallization are discussed in greater details in Chapter 3.*

2.4.1. Standard Al-BSF solar cell

The majority (~90%) of crystalline Si (c-Si) solar cells manufactured today are based on two side contacted solar cells [ITR13]. Traditionally, the PV industry uses p-type (boron) doped wafers due to the simplicity of creating the n^+ doped (phosphorous) emitter layer and the p^+ back surface field (BSF) by aluminum (Al) alloying (so-called standard Al-BSF solar cells).

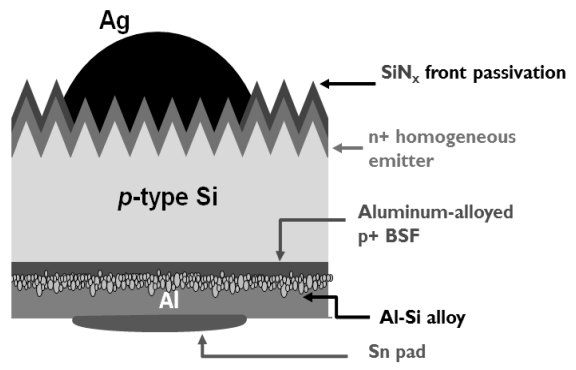
Al-BSF solar cells are essentially a 30 years old concept. The concept of reducing minority carrier recombination at the rear side by introducing a high-low p/p^+ homojunction at the rear surface was first introduced in c-Si solar cells by Mandelkorn et al. in 1973 [MAN73]. Consequently, the first printed and fired contacts were demonstrated in 1975 by Ralph [RAL75] and Frisson et al. in 1978 reaching energy conversion efficiencies around 12% [FRI78]. Since 1978, process and equipment for the screen-printed Al-BSF solar cells has been further optimized and new technologies have been introduced. (i) Plasma enhanced chemical vapor deposition (PECVD) silicon nitride as an antireflection coating with excellent surface and bulk passivation properties [DUE02]. (ii) Texture of the front surface to reduce reflection of mono- and multicrystalline silicon [KIN91, EIN97]. (iii) Single-side etching/polishing for the electrical separation of the front and rear contacts [DEL04, RAP12]. (iv) Various selective emitters

technologies (n^{++} under the front contacts, n^{+} in between) leading to better short wavelength response ("blue-response") and improved fill factors [HAH10]. (v) New interconnection technology enabling the suppression of rear silver pads leading to reduced cost and improved performance [VON12]. (vi) improved Al-BSF properties thanks to boron doping of screen printed Al pastes [RAU13]. (vii) Improved silver paste formulations enabling fine line printing and contacting of lowly doped homogeneous n^{+} emitters [MUS13]. Today's best Al-BSF solar cells reach energy conversion efficiencies up to 17.9% and up to 19.9% on large area (243 cm^2) multi-crystalline (mc-Si) and Czochralski mono-crystalline Si (CZ-Si) [MET13].

One example of an Al-BSF process is presented for p-type CZ-Si and a cross-section schematic of the resulting cell are in Table 2.3. 15.6x15.6 cm^2 wafers are wire sawn from a p-type CZ-Si ingot resulting in wafer thicknesses in the range of 150-200 µm. The wafers are chemically cleaned. Damage resulting from the sawing process is removed while texturing the surface to reduce front side reflection using an alkaline solution which is then neutralized in a HF/HCl solution to prevent contamination [KIN91]. The wafer surface is then diffused in a tube furnace at 800-900˚C in a $POCl_3$ atmosphere resulting in a n^{+} emitter with a sheet resistance R_{sh}~ 80-100 Ω/sq and a surface dopant concentration around $1x10^{20}$ cm^{-3}. Consequently the parasitic rear n^{+} emitter is removed in an inline single side etching tool also removing the phosphosilicate glass (PSG). This step can also be combined with rear surface polishing to reduce minority carrier recombination at the rear. A PECVD hydrogen rich silicon nitride (SiN_x:H) anti-reflection coating is applied at the front. A front H-pattern grid and a blanket rear contact are applied using screen printing of a silver containing and aluminum containing paste respectively (for more details on screen printing see chapter 3). The two side metal-silicon contacts are created simultaneously during a fast co-firing step (T>700˚C for a few seconds) in a belt furnace. During the firing step, the Al-alloyed p^{+} BSF is formed and hydrogen is released from SiNx:H leading to reduced surface and bulk recombination. Rear soldering pads (Tin Pad) are applied using ultrasonic soldering [VON12]. Finally the wafers are measured (I-V measurement) and sorted.

Table 2.3: Example of an Al-BSF process for p-type CZ-Si (left-hand), schematic of the resulting cell (right-hand).

1) Random pyramid texture (KOH bath)
2) POCl3 diffusion +PSG removal
3) Parasitic rear emitter removal
4) PECVD SiN_x:H front
5) Ag screen printing front (H-pattern)
6) Al screen printing rear (blanket)
7) Co-firing
8) Rear soldering pads (Tin Pad)
9) I-V measurement and sorting



2.4.2. Advanced cell structures

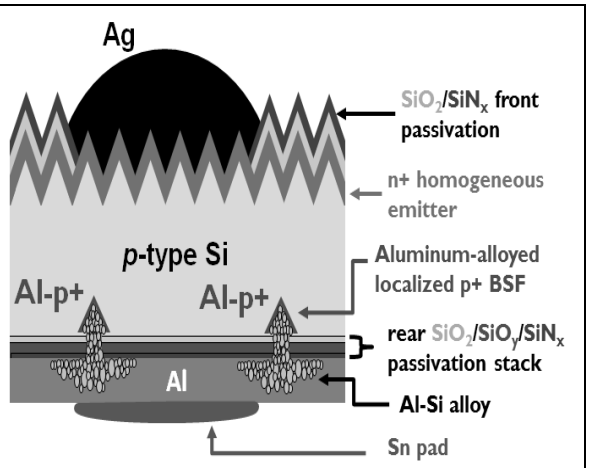
Standard p-type large area Al-BSF solar cells are limited by: i) optical and recombination losses at the rear surface, ii) front shading losses, and iii) reduction of minority carrier lifetime upon illumination (light-induced degradation) [PAL07]. Several advanced solar cell structures have been proposed to tackle those three points. Due to the strongly on-going reduction in wafer, cell and module manufacturing costs these new structures need to: i) be simple (few extra steps, high throughput) and ii) show significant efficiency improvement over p-type Al-BSF solar cells.

Dielectric rear surface passivation allows to potentially overcome both carrier recombination and parasitic light absorption at the rear surface of Al-BSF solar cells at once. Passivation of the rear surface by a dielectric layer deposited by PECVD was first presented by Jäger and Hezel in 1986 in combination with local evaporated contacts [JAG86]. In 1989, the first so-called "passivated-emitter and rear cell" (PERC) was presented by Blakers et al [BLA89]. In the original PERC concept, local contacts in the rear dielectric passivation were defined by photolithography followed by a full-area metallization on the rear serving as contact and improving internal rear reflectance. As minority carrier recombination at the local rear contacts was found to limit the performance, the same group proposed to use an oxide mask patterned by photolithography to form locally a boron diffused back surface field under the contacts. This cell structure is called "passivated emitter, rear locally diffused" (PERL) type solar cells and lead to world record 25% energy conversion efficiency at 1 sun irradiance [ZHA99]. However, in this PERL cell dielectrics layers were formed using relatively thick thermal oxide. The (inverted pyramid) front texture and the (evaporated) front and rear contacts were defined by photolithography. As all these processes were not suited for mass production, industrial PERC (i-PERC) also referred to as local back surface field (LBSF) solar cell structures were developed.

In the i-PERC process as proposed by Agostinelli et al. in 2005 [AGO05], the thick thermal oxide at the rear is replaced by a stack of oxide, deposited by atmospheric-pressure CVD (APCVD), and PECVD silicon nitride. A thick SiO_y oxide layer (>100 nm) is required to prevent fixed positive charges in the silicon nitride to cause a floating junction at the rear degrading cell performance and to maintain efficiency gains over standard Al-BSF. Subsequently, contact holes are formed by laser ablation instead of photolithography and a local Al-BSF is formed at the contact holes by screen printing (or evaporation/sputtering) an aluminum layer which is subsequently co-fired with the front Ag grid. An example of i-PERC processing sequence as performed at imec is given in Table 2.4. A low temperature thermal oxidation is introduced prior to PECVD deposition to reduce surface recombination and improve the fill factor [PRA13]. With the exception of cleaning steps which might be performed prior to $POCl_3$ diffusion and prior to thermal oxidation, this i-PERC sequence introduces three extra steps compared to the Al-BSF sequence given in Table 2.3. Efficiencies up to 20.3% were achieved at imec on 15.6x15.6 cm^2 CZ-Si using screen printed Ag contacts. In this thesis, efficiencies up to 20.8% were achieved on i-PERC p-type 15.6x15.6 cm^2 solar cells using Ni/Cu plated contacts at the front.

Table 2.4: Example of an i-PERC process for p-type CZ-Si sequence (left-hand) and a cross-section schematic of the resulting cell (right-hand).

1) Random pyramid texture (KOH bath)
2) $POCl_3$ diffusion + PSG removal
3) Parasitic rear emitter removal
4) Low temperature thermal oxidation
4) PECVD SiN_x:H front
5) PECVD SiO_y/SiN_x:H rear
5) Laser ablation rear (contact holes)
5) Ag screen printing front (H-pattern)
6) Al sputtering
7) Co-firing
8) Rear soldering pads (Tin Pad)
9) I-V measurement and sorting



As the i-PERC process makes use of a relative thick dielectric stack, different processing sequence and different dielectric layers were introduced. One example of alternative processing sequence is laser fired contact (LFC) solar cells [PRE00]. In the LFC process sequence, Al is first deposited on top of the rear dielectric stack and co-fired with the Ag front grid. Only subsequently the rear contacts are formed by locally melting Al to penetrate the dielectric stack and form the local back surface field (LBSF) regions. Another example is the PLUTO-PERL sequence where locally boron diffused regions are created by applying a dopant source (typically spin-on dopant) on top of the rear dielectric and using a laser to incorporate boron in silicon by local melting prior to real Al evaporation. Using this sequence in combination with a laser doped selective emitter and plated Ni/Cu contacts at the front extremely high j_{sc} values up to 40.9 mA/cm^2 values were obtained demonstrating the strong potential of PLUTO-PERL [WAN12]. Finally, since 2008, Aluminum oxide (Al_2O_3) usually in combination with PECVD SiNx:H emerged as a strong candidate to replace the thick PECVD SiO_y/SiN_x:H stack at the rear [HOE06, SCH08, VER12b, CAS12]. Al_2O_3 contains a high density of fixed negative charges thereby eliminating the risk of floating junction on p-type. In addition, it offers excellent passivation properties using extremely thin (<10 nm) and uniform layers which can quickly be deposited using spatial atomic layer depositions tools or PECVD systems [VER12b, CAS12]. The application of Al_2O_3/SiN_x:H rear passivation stacks on homojunction large area (243 cm^2) p-type LSBF type solar cells lead to record energy conversion efficiencies up to 21% and 21.3% using screen printed Ag and Ni/Cu plated front contacts respectively [MET13]. In this thesis, efficiencies up to 20.7% were obtained on p-type 15.6x15.6 cm^2 with Ni/Cu front contacts.

Unlike standard boron doped CZ-Si, n-type CZ-Si does not suffer from light induced degradation. N-type material offers superior minority carrier lifetime than p-type for the same defect concentration leading to much greater diffusion lengths [MAC04]. The high diffusion lengths enable the use of rear junction cells where the p^+ boron doped emitter can be moved from

the front texture side to the planar rear side leading to reduced recombination as shown by Dai et al. [DAI93] with the passivated emitter and rear totally diffused (PERT) cell structure. Using this n-PERT structure and Al_2O_3 for the passivation of rear p+ emitter, record efficiencies up to 21.3% have been demonstrated on 15.6x15.6 cm^2 n-Cz Si [MER13]. In this work, efficiencies up to 20.7% were demonstrated when using Ni/Cu plated front contacts in an n-PERT cell structure.

2.4.3. PV Module fabrication and IEC testing

As a solar cell is a source of DC electric current with a low DC voltage (V_{mpp}~0.5-0.6 V), it is required to interconnect a large number of cells in series in a module to achieve a large enough DC voltage that in turn may be converted into AC using an inverter. It is important that novel cell concepts developed in this thesis can undergo photovoltaic (PV) module fabrication. PV module fabrication and IEC standard testing are briefly introduced here.

Conventional PV module

Solar cells are typically interconnected in series by means of tinned (typically Sn/Ag/Pb) copper ribbons (typically 2 mm wide and 0.2 mm thick) which are continuously (or in spots) soldered onto the front busbar of the cell and from then onto the rear busbar pads of the next cell forming a string of cells. Strings are then interconnected in series by means of tinned copper bussing (wider ribbons). If one cell is shaded in a string, the remaining cells force the shaded cell in reverse voltage driving through the cell. Since the shaded cell acts as a resistor, this might result in a local heating (hot spot) of the cell which might ultimately destroy the module. To prevent this by-pass diodes are included across the PV strings causing the entire string to switch off if one cell is shaded. Typically, modules are fabricated using 6 strings of 10 cells.

Since PV modules are required to operate for more than 20 years without degradation their fabrication must withstand various weather conditions. Typically, this involves the use of transparent low-iron tempered sheet of glass at the sunny side of the strings. The strings are sandwiched between sheets of encapsulant material (typically ethylene vinyl acetate: EVA) and a reflective back sheet (typically Tedlar® from DuPont) is added to prevent penetration of moisture. Holes are made through the backsheet and EVA so that the strings and by-pass diodes can be later on connected to an external junction box. The stack of glass/EVA/strings/EVA/Tedlar is then vacuum laminated at 140-160˚C to build a strong bond between the layers free of air-bubbles. An aluminum frame is then mounted at the perimeter of the glass sheet to protect against damage, provide mechanical support, and facilitate mounting.

Advanced PV module fabrication

Conventional PV module fabrication introduces additional cell-to-module optical and electrical losses (mainly Fill Factor). Optical losses are reduced in advanced PV modules, by making use of i) high transparency textured glass coated with an anti-reflection coating, ii) UV-transparent encapsulant such as silicone, iii) increased reflection from the back sheet by leaving gaps between the cells, and iv) V-grooved ribbons reducing the reflection loss at the busbar [MET13]. Fill factor losses are caused by the fact that the current needs to pass through the narrow (~2 mm) ribbons. Using wider ribbons as well as using more ribbons of the same width introducing shading losses and using thicker ribbons introduces more stress and risk of cracking the cells. For two-side contacted solar cells, FF losses are reduced by using an increased number of narrow busbars or Cu coated wires instead of ribbons.

IEC standard testing

It is common practice in the market to sell PV modules covered by a 20+ year warranty. The warranty is supposed to cover safe operation (no electrical, thermal, mechanical and fire hazards) and limited power output degradation. The industry has defined a performance standard (IEC 61215) for c-Si modules. It is important to mention that the IEC6125 standard is not a reliability standard and hence does not imply the module will last over 20 years in the field.

The IEC61215 standard testing includes visual inspection, electrical safety, performance (P_{max} at standard testing conditions, P_{max} at low irradiance, temperature coefficients), irradiance (e.g. UV exposure), environmental, and mechanical (e.g. mechanical load, hail impact) tests. Typically the most stringent tests are the environmental tests which consists in temperature cycles from -40˚C to +85˚C (TC200), humidity freeze (HF), and damp heat (DH) testing in 85% relative humidity. TC200 in combination with DH testing can account for up to 70% of failure rates for c-Si modules [ARN13]. This is because of the different thermal expansion coefficients between Si, metal contacts, and the Sn/Ag/Pb copper ribbons inducing a high amount of stress on the wafers. A high degree of stress might lead to front grid delamination or wafer breakage causing a major loss in P_{max}. In addition, mechanical cracks introduced during soldering might lead to failure during TC or DH testing. As the thesis deals with the implementation of nickel/copper contacts as an alternative to silver screen printing for the front side metallization of industrial high efficiency silicon solar cells, it is required to demonstrate that cells with such contacts can pass TC and DH testing. This is discussed extensively in Chapter 7 which is dedicated to the reliability of Ni/Cu contacts.

CHAPTER 3

Front side metallization of Si solar cells

As this thesis deals with the development of nickel/copper (Ni/Cu) plated contacts as an alternative to silver (Ag) screen printing for the front side metallization of silicon solar cells, it is important to introduce industrial screen printing. This is done in section 3.1 where we take a look at the limitations and the resulting pressure to innovate. Section 3.2 describes advanced printing techniques. Alternative metallization concepts based on the concept of seed and plate are introduced in section 3.3 with an emphasis on technologies enabling the use of Cu. Competing metallization concepts at module level are discussed in section 3.4. The approach chosen in this thesis and challenges to overcome for industrial adoption are given in section 3.5. Further details beyond that can be found in review papers on this topic [GLU07,EBO12] as well as PhD thesis on front metallization of Si solar cells, in particular [SCH06, MET07, HOR09a, BAR12] for Ag based contacts and [TJA10, SUG11, BAR12, ALE13] for Cu based contacts.

3.1. Industrial screen printing

3.1.1. Principles of screen printing

Screen printing is a rather simple process where to create a desired pattern, the printed metal-containing paste is pushed through a patterned screen with the help of a squeegee. Screens, are typically made of a mesh of stainless steel (high tensile strength) wires which are clamped at the perimeter to an aluminum (Al) frame on which a photo-sensitive emulsion layer is deposited and patterned by photolithography (see Figure 3.1a). For the front side metallization, it is desired to form narrow fingers thus narrow openings are defined in the emulsion (Figure 3.1b).

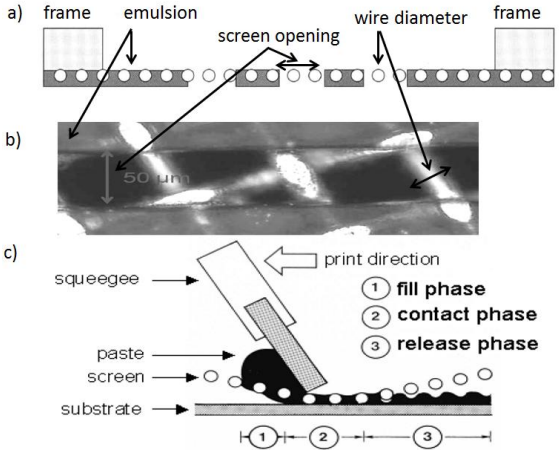


Figure 3.1: a) Schematic of a screen design (cross-section), b) Optical microscope picture of a screen taken from [MUS13]. c) Schematic of the screen-printing step consisting of 3 consecutive phases, taken from [MET07].

The printing step can be categorized in three consecutive phases (Figure 3.1c). During the fill phase, the opened areas are flooded by the paste which is moving in front of the squeegee. During the contact phase, a vertical force is applied to the squeegee bridging the vertical distance between the substrate and the screen and forcing paste through the screen openings. As the squeegee moves forward the paste which is sticking on the substrate is released from the screen.

The printing result depends on many factors that include screen parameters, printing parameters, and paste composition/rheology [MET07]. For the metallization of standard Al-BSF solar cells (see section 2.3.1) at least two printing steps are performed to define the front (typically silver (Ag) containing paste) and rear contacts (typically Al containing paste). Ag is used because it is the best electrical conductor (ρ_{Ag} = 1.61 μΩ.cm). Less conductive metals such as copper, nickel, or zinc have been shown to be incompatible with a high temperature firing through process [RUD13]. Latest generations of screen-printing industrial are capable of maintaining throughputs ~2700 wafers/hour by using parallel printing stations.

3.1.2. Silver pastes and contact formation

Silver containing pastes used for the front side metallization of silicon solar cells typically consists of μm size Ag particles, glass frit, solvents, and organic binders [MET07]. These components define the rheological behavior, contact resistance, line resistance, and adhesion properties of the contacts. Contact formation is done by sintering the wafers in a fast firing belt furnace where the substrates are quickly heated to ~800˚C. Solvents are evaporated ~300˚C and organic binders are burned out between 300 and 500˚C. The glass frit (typically containing ~10% of lead oxide PbO) wets and etches the SiN_x anti-reflection coating in a series of Redox reactions causing PbO to be reduced and Si to be oxidized forming a SiO_y layer at the interface. The PbO silicate glass helps liquefy Ag far below its melting point and transport it to the Si surface where Ag and Pb can form different phases which solidify upon cooling. A full overview of contact formation processes are given in [HOR09a] while the influence of the front side texture on the Ag crystallites density is discussed in [CAB11, LAU11a]. At the rear side, Si is dissolved into liquid Al and re-crystallizes epitaxially upon cooling leading to the back surface field (BSF) p^+ formation (see section 2.3.1). An overview of Al-BSF formation is given in [HUS05] and local Al-BSF formation in i-PERC solar cells is discussed in [URR12, URU13a].

Silver pastes underwent a tremendous amount of optimization in the recent years. The sintering behavior was improved to achieve denser and more conductive fingers [LAU11a, MUS13]. The wetting/etching behavior was enhanced to give uniform SiN_x:H removal and ultra-thin glass formation at the interface [LAU11a], The rheological behavior was tuned leading to narrower finger widths with improved uniformity and higher aspect ratio (width to height ratio) [LAU11a, MUS13]. Adjustments in the composition enabled to contact lowly doped emitters [LAU11a, MUS13, KAL13]. Such progress made possible to reach efficiencies up to 21% on large area (243 cm^2) LBSF p-type solar cells featuring a 100-110 Ω/sq homogeneous emitter [MET13, LAC12] which were unthinkable of a couple of years ago (compare Figure 3.5).

3.1.1. Fine line printing

In order to achieve narrower finger widths, numerous front side metallization technologies have been evaluated. These technologies are similar to screen printing regarding the contact formation process except the composition/rheology of the paste might be adapted. Technologies mentioned here enable printing of relatively thick (>5 µm) films in one printing step and are currently being considered for mass-scale production. Other technologies (ink-jet printing, aerosol jetting, etc.) typically leading to thinner layers are discussed in section 3.2.

Stencil printing was first envisaged for fine line printing in production in 1998 [HOO98]. The advantage of stencil printing over screen printing lies in the improved paste release, non-wear character of the stencil, and the ability to print fingers with high aspect ratios. Stencils can be categorized into single layer stencils or double layer (also called hybrid) stencils [HOO09]. In both cases the opened fraction is much higher than with conventional emulsion screens In single layer stencils, as shown in Figure 3.2b, the open fraction is 100% and hence a second printing step is required to print the busbars (often referred to as dual printing). In a double-layer stencil, as shown in Figure 3.2c, the fingers and busbars are fully opened in one layer while in the other connections are made between fingers and busbars to prevent the stencil from falling apart. There has been excellent results published with stencil printing with 35 µm (height: 14 µm) and 61 µm wide fingers (height: 17.4 µm) obtained with single layer and double layer stencils respectively [FAL11]. However, industrial adoption has been limited, mainly because of recent progress made using emulsions screens and also due to the fact that the manufacturing of stencils remains expensive (particularly for double layer stencils). Nevertheless, dual printing using single layer stencils is gaining momentum as it enables drastic reduction in Ag consumption and efficiency gains when combined with a non-firing through Ag paste for busbars printing [MUS13, KOS13, HAN13]. Another approach is Print-on-Print (also called double printing) where a second layer of paste is screen printed on top of the first one [GAL10].

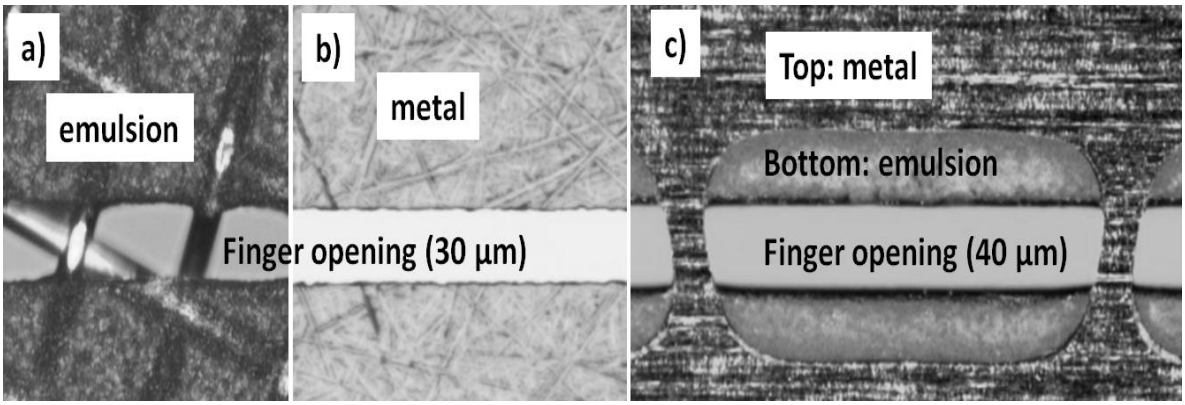


Figure 3.2: a) Emulsion screen with 30 µm opening, 380 mesh, and 14 µm wire diameter. b) Single layer electroformed nickel stencil with 30 µm opening. c) Hybrid stencil with 40 µm opening, stainless steel at the top is chemically etched and bottom emulsion layer (paste side) is patterned by photolithography. Taken from [FAL11].

3.1.3. Limitations and pressure to innovate

The co-optimization of screen design, printing parameters, and printing pastes has been key to push the limits of industrial screen printing. However, despite these improvements screen printing of Ag for the front side metallization of silicon solar cells presents intrinsic limitations.

The current trends with screens involve using narrow opening width (state-of-the-art: 45-60 µm), smaller wire diameter (state-of-the-art: 18 µm), and high opening fractions [MUS13, FAL11]. However, this reduces the screen lifetime (faster loss of tension, screen breakage) and leads to higher risks of finger interruptions (particularly with more viscous Ag pastes) and higher finger resistance as the printed amount is reduced. On the other hand, more advanced fine line printing techniques often require expensive screens and make use of two printing steps which leads to higher yield losses (alignment needed, wafer breakage). All these factors limit screen printing up-time and limit further reductions in solar cell manufacturing costs.

Despite, progress made in the recent years with screen printed Ag pastes, there is a general consensus that Ag pastes are limited to surface concentrations (N_s) around $1x10^{20}$ cm^{-3} on phosphorous doped emitters [BEA12] which are not ideal in terms of recombination [SAN09]. Using selective emitters to optimize separately the contacts and the emitter introduces extra steps/complexity (cost increase) and also requires high alignment accuracy [HAH10]. Firing Ag paste is a high temperature process which when combined with aluminum rear contact formation leads to a reduction in internal rear reflectance and hence in cell efficiency [WAN12]. Finally, Ag is an expensive and noble material and hence is subjected to high price volatility, as shown in Figure3.3a, particularly since the demand for Ag in other industrial applications (automotive, portable electronics) is foreseen to increase in the future [THE12].

The photovoltaic industry has recognized that metallization pastes containing silver (Ag) and aluminum (Al) are the most process critical and expensive materials in current cell technologies besides the wafer itself [ITR13]. In February 2013, Ag alone represented 1/3 of total cell processing costs for an Al-BSF solar cell on p-type m-Si as shown in Figure 3.3b.

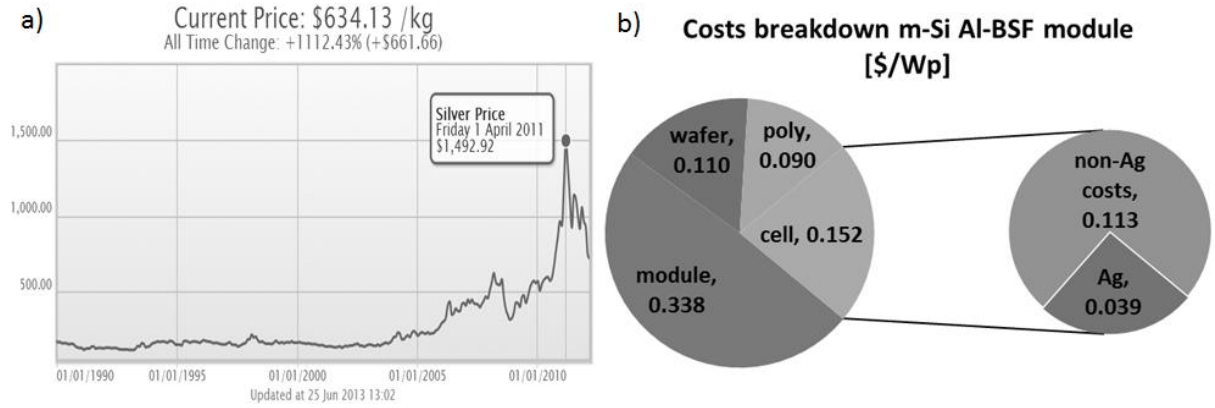


Figure 3.3: a) Silver (Ag) price in $/kg since 1990 [source: www.bullionbypost.co.uk, 25/01/13]. b) Costs breakdown of a multi-Si (m-Si) Al-BSF module in $/Wp assuming 4.13Wp (eta~17.0%), Ag: $800/kg with 0.2g/cell. [ITR13]

Despite the current lower silver prices, the PV industry acknowledges that reducing Ag consumption is a mandatory step towards reducing costs. Expected developments of silver amount used per cell in mass-scale production are shown in Figure 3.4. Interestingly, the decrease in Ag consumption over the last two years happened faster than expected demonstrating the pressure on reducing costs. On the other hand, the decreased in wafer thickness (to reduce silicon costs) occurred slower than expected due to the strong reduction in silicon prices experienced in the recent years and the difficulty to handle thin wafers in current production tools without experiencing increased yield losses. Nevertheless, looking at 2017 and beyond, further reducing Ag consumption to 50 mg/cell requires alternative metallization techniques enabling very efficient use of Ag or enabling the replacement of Ag by another conductive metal. An obvious candidate for this is copper (Cu) since it is >100x cheaper per kg than Ag and almost equally as conductive (ρ_{Cu} = 1.67 μΩ.cm). In addition, these alternative metallization techniques must be compatible with thin wafers and cell efficiencies > 20% as shown in Figure 3.5.

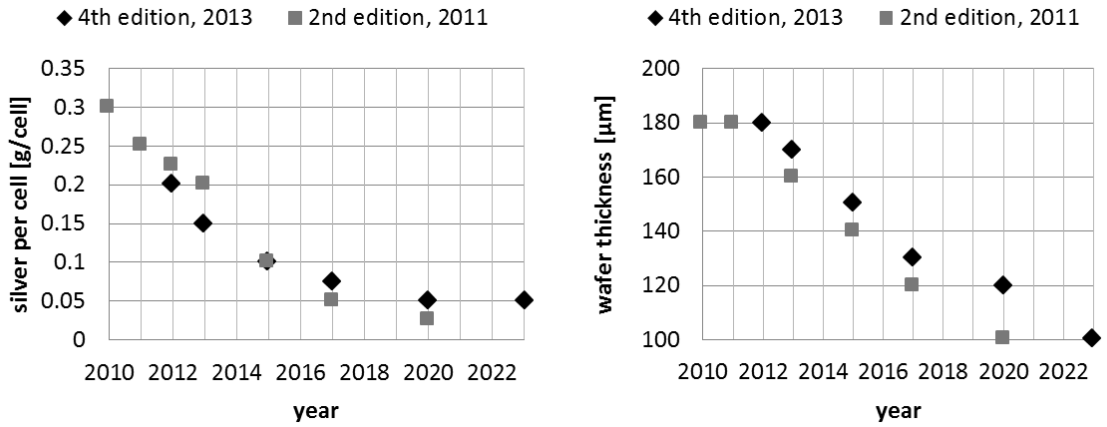


Figure 3.4: Expected developments of silver amount used per cell (15.6x15.6 cm^2) and of wafer thickness in solar cell mass-scale production based on 4th (published in 04/2013) and 2nd (published in 04/2011) editions of International Technology Roadmap for Photovoltaic (ITRPV) [source: www.itrpv.net, 04/01/2013].

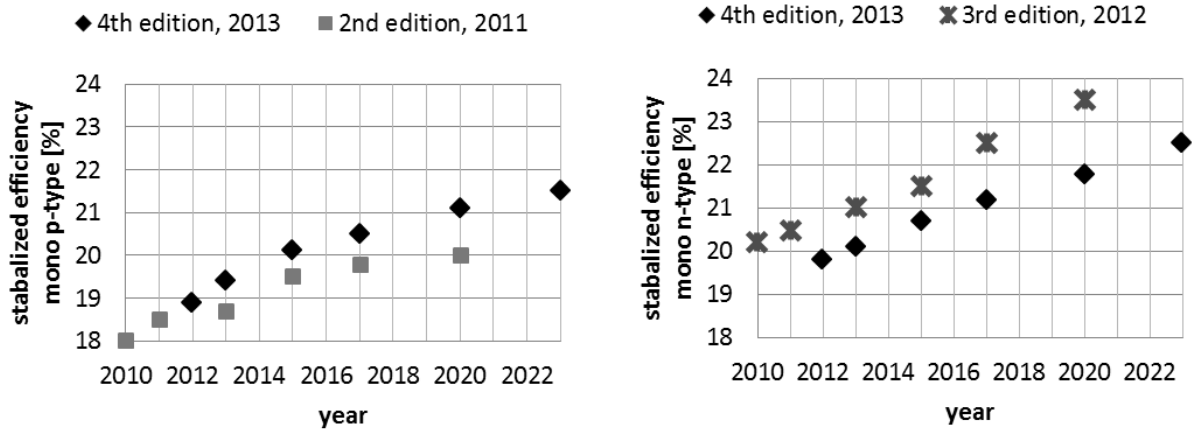


Figure 3.5: Expected developments of stabilized efficiency on mono p-type and n-type Si in mass-scale production based on 4th, 3rd, and 2nd editions of ITRPV [source: www.itrpv.net, 04/01/2013].

3.2. Alternative front side metallization techniques comprising two or more layers

Alternative front side metallization techniques to screen printing of silver are based on the concept that by using two (or more) layers, the contact formation and the lateral conductivity of the front grid can be optimized separately. Such a "seed-and-plate" concept allows the use of Ag or Cu plated layers which offer better conductivity than screen printed Ag layers and hence enable drastic reductions in Ag consumption. Front side metallization techniques mentioned here include process sequences used historically for high efficiency small area cells as well as well as techniques envisaged for mass-scale production. An emphasis is given on techniques enabling the use of Cu. Diffusion barrier requirements for Cu plated layers are discussed in section 3.2.4.

3.2.1. Metallization of high efficiency small area cells

In solar cells for space, concentration, or laboratory applications, it is more critical to limit losses caused by the front metallization rather than achieving a high-throughput low-cost process. Therefore, ultra-fine lines are defined using a lift-off metallization sequence as shown in Figure 3.6 where contact opening, contact resistance, and line resistance are separately optimized. Narrow contact openings (typically 5-10 μm wide) are formed by photolithography patterning and wet chemical etching (no damage in silicon). Following this a stack of metal is deposited at the front (typically by thermal/e-beam evaporation). A common stack of metal is titanium-palladium-silver (Ti/Pd/Ag) using Ag as the main conductor since it is the most conductive metal. Ti presents the advantages of reducing native oxide, giving good adhesion to silicon, and enabling low specific contact resistance values on lowly doped emitters (ρ_c< 1E-5 $\Omega.cm^2$ for N_s>1x10^{19} cm^{-3}). Pd is used as diffusion barrier (particularly against oxygen) and adhesion promoter between Ag and Ti. For the lift-off sequence, solvents (typically acetone) are used as they penetrate into the thin (or absent) metal layer at the edges of the opening and dissolve the photoresist lifting-off the metal on top. Finally the contact stack is sintered at temperatures below 500˚C to improve contact properties.

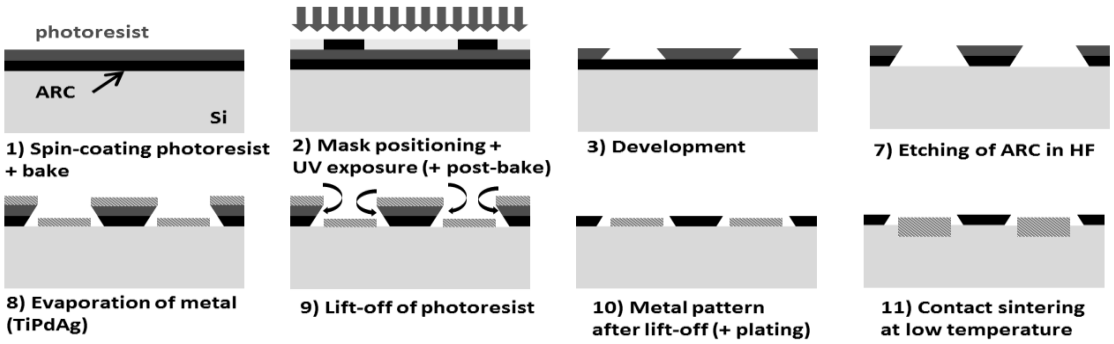


Figure 3.6: Metallization sequence based on photolithography patterning of the anti-reflection coating, metal deposition (evaporation or sputtering), and lift-off. Post-bake step and slope in photo-resist after development depend on photoresist used, post bake conditions, and UV exposure conditions. An additional thickening step by plating might be performed after lift-off to increase finger conductivity (see section 3.2.4).

3.2.2. Concept of seed and plate

Large area solar cells need relatively thick fingers to transport the current to the busbars. On the other hand, evaporation/sputtering processes deposit metals at relatively slow rates and the thicker the metal stack the more difficult it is to perform a lift-off sequence.

In 1957, investigations on creating ohmic contacts to n- and p-doped silicon using electroless nickel (Ni) plating solutions were published by Sullivan and Eigler [SUL57]. In 1962, Mandelkorn et al. [MAN62] combined photolithography patterning and electroless Ni plating to define the front side contacts of silicon solar cells. The nickel contacts were subsequently covered by solder by dipping the wafer into a molten solder bath to improve finger conductivity and solderability. This is the first example of "seed-and-plate" approach where a conductive layer is deposited on top of a pre-deposited metal layer (or stack). The first metal layer (or stack) is also called 'seed" layer and should have a low contact resistivity. The second metal layer should have high conductivity and can be deposited by plating.

The combination of evaporated and plated contacts in a seed-and-plate approach is widely used for high efficiency small area cells (space, concentrator, laboratory) where a stack of Ti/Pd/Ag is first deposited using a lift-off sequence and subsequently Ag plated. This sequence offers all required technological properties for the front side metallization (solderability, reduced shading loss, high conductivity, low contact resistivity, good adhesion to silicon, and long-term stability). Using 7 μm wide seed layers, the Ag plating step only takes a few minutes to get semi-roundish fingers with 20 μm physical widths and 10 μm optical width (light is reflected back into the wafer) [BAR12]. Over the years, considerable efforts were made to achieve dense and highly conductive Ag plated layers using cyanide-free solutions [MET07, HOR09a, BAR12]. Various evaporated seed layer stacks (Ti/Pd/Ag, Ti/Ag, Cr/Ag, Ni/Ag, Al/Ag, Pd/Ag) were compared by Mette for different sintering temperatures [MET07]. He concluded that laboratory cells featuring Ni/Ag and chromium-silver (Cr/Ag) front side contacts could deliver efficiencies comparable as laboratory cells featuring the reference Ti/Pd/Ag stack. He also mentioned that further adhesion tests, long term stability tests, and damp heat tests should be conducted. However, an approach based on photolithography patterning is not economically feasible in mass-scale production due to the number of steps (see Figure 3.6) used for the seed-layer definition.

3.2.3. Seed layer formation using fine line printing

Seed-and-plate concepts based on seed layers deposited using fine line printing can be seen as an evolutionary approach from screen printing. Contact formation still relies on firing through a Ag paste but the finger conductivity is obtained from a subsequent Ag plating step.

Early developments of this approach consisted in depositing a narrow seed layer using emulsion screens or stencils followed by a short light-induced plating (LIP) step of silver to "augment" the paste conductivity (see section 3.2.3 for details on LIP). It presented the advantage of using well-known high throughput processes for the seed layer deposition. In

addition, the LIP step was shown to lower contact resistance of the printed seed layer which together with reduced shading and finger resistance losses lead to 0.3-0.4% absolute gain in efficiency [MET07]. An extension of the contact model for screen printed and plated contacts was proposed introducing new possible current flow paths at the edge but also in the center of the finger [PSY09]. Similar improvements of the contact resistance were reported even for short plating times and attributed to the thinning of the glass layer in the LIP solution [EBO08].

A second approach is to use seed layers depositing by contactless techniques which are well suited for the metallization of thin wafers. A comprehensive review of contactless (also called direct-writing) techniques is given by Hon et al. [HON08]. Among these techniques, aerosol-jet or ink-jet printing were shown to enable the deposition of very narrow metal fingers (below 20 μm wide) [MET07]. Layers deposited are very thin (typically few μm or less) and can be optimized solely for their contact properties since the conductivity is obtained from the subsequent Ag plating step. In aerosol printing, the paste is atomized into an aerosol and focused through a nozzle using a sheath gas. Conventional Ag particles (~1-10 μm in size) can be passed through the nozzle without risks of clogging. Major developments in the formulation of inks for aerosol printing have been done in order to achieve low contact resistance on lowly doped emitters [HOR09a, KAL13]. Most notably, Horteis et al. [HOR10a] reported that, using fired aerosol printing seed layer and a subsequent Ag plating step, they could contact a 110 Ω/sq emitter resulting in an efficiency of 21.1% on 4 cm^2 float-zone Si. Ink-jet printing makes use of Ag inks to form droplets that fall onto the substrate. The achievable finger widths are determined by the droplet volume. Therefore, dedicated inks consisting of nano-sized Ag particles with a low metal content (very low viscosity) are required since the ink needs to pass through narrow nozzles. This technique presents the advantage of precise control since each nozzle can be addressed separately to generate a droplet on-demand using a piezoelectric membrane. Ebong et al. [EBO10] described the use of an XJET ink-jet production tool capable of processing 2400 wafers per hour. Seed-and-plate results in pilot production using the XJET tool, a high-throughput aerosol tool, and screen printing for the seed layer were compared by Mette et al. [MET12]. However, despite their respective advantages, both aerosol and jet-printing have had difficulties to find their way to mass-scale production. This is mainly because of progress made with screen printing together with new pastes available for lowly doped emitters (see section 3.1). This resulted in a reduced interest in seed-and-plate concepts based on silver plating.

A third approach is to use copper (Cu) plating on top of a Ag seed layer deposited using fine line printing techniques. The advantages of such an approach is that the contact formation is based on a well-known process (e.g. aerosol-jet, Ag firing-through paste) and material costs can be reduced thanks to the use of Cu [KAM11]. However, since Cu diffuses fast into silicon and is detrimental to solar cell a barrier layer is required between the Ag seed layer and Cu [BAR10]. A capping layer is also required on top of Cu to prevent Cu from oxidizing and from reacting with the encapsulant material. However, this approach presents numerous disadvantages since it increases complexity (4 metal layers), leads to adhesion issues between the seed layer and the plated layers, and remains limited by the contact properties of the seed layer.

3.2.4. Copper diffusion in silicon

Copper is known since the 1960s to be very detrimental to minority carrier lifetime in silicon and hence the decision of IBM to introduce in 1997 Cu based interconnects in the production of their integrated circuitry (IC) chips is very insightful [AND99].

Copper is the fastest diffusing 3d transition metal in Si as shown in Figure3.7a. Cu diffusion in Si occurs via interstitial diffusion of Cu^+ which means that the diffusivity of Cu depends not only on temperature but also on the doping type and doping level of the sample [KOH09]. Since Cu^+ diffuses very fast even at room temperature, it is not stable in the interstitial state and forms precipitates or complexes. A fraction of these precipitates form electrically active levels in the band gap that act as minority carrier recombination sites (Shockley-Read-Hall recombination, see Chapter 2.1.3) and hence Cu is also known as a "lifetime-killer". The effect of Cu, iron (Fe), and nickel (Ni) on minority carrier lifetime in CZ-Si is shown in Figure 3.7b which clearly illustrates that even extremely low surface contamination levels ($1x10^{11}$ cm^{-2}) can be detrimental. Fe is the most detrimental impurity in Si because of the strong recombination activity of interstitial Fe and of Fe-boron pairs [IST98]. In n-type Si, Ni and Cu are as detrimental as Fe because of the higher capture cross section for holes than for electrons of Ni and Cu-related precipitates. Importantly, the recombination activity of these precipitates depends on the presence of nucleation sites and other types of defects inside the material (e.g. grain boundaries in multi-Si) which can strongly be influenced by thermal treatments (see oxygen precipitates in CZ-Si in Chapter 5).

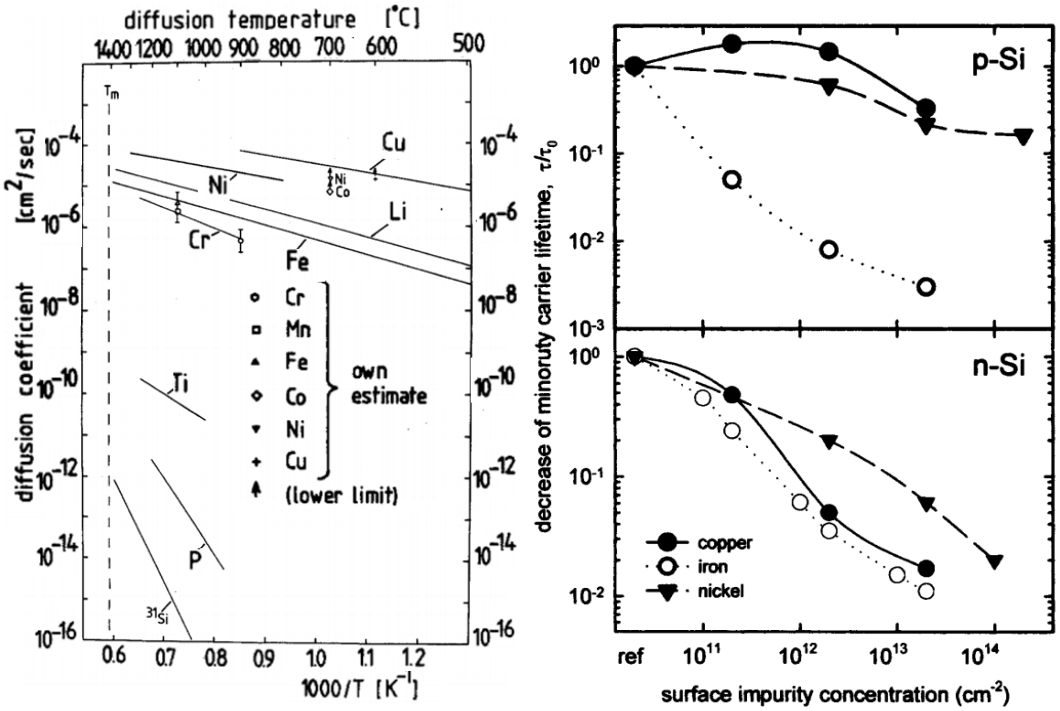


Figure 3.7: a) Diffusion coefficient versus temperature for 3d metals in silicon [WEB83] b) Normalized minority carrier lifetime in p- and n-type CZ-Si versus surface concentration of copper, nickel, and iron [IST98].

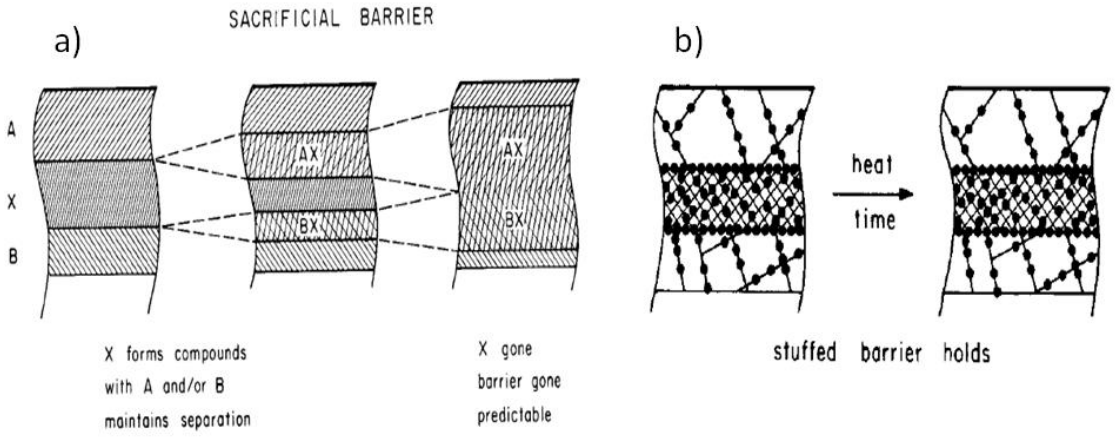


Figure 3.8: a) Sacrificial barrier X between A (e.g. Cu) and B (e.g. Si) b) Stuffed barrier: impurities along grain boundaries hinder Cu diffusion, Taken from [NIC81].

The decision of IBM to introduce in 1997 Cu plated interconnects in production changed dramatically the IC industry as it quickly became the standard technology [AND99]. This is because not only IBM had solved issues related with Cu but also because they could benefit from higher performance and lower processing costs than with the previous Al interconnects. For instance, a capping layer is required to prevent Cu from corrosion as copper oxides are readily formed at temperatures above 100˚C and do not form a protective layer (unlike Al_2O_3 with Al) [KOH09]. As the dimensions in IC chips keep shrinking, very effective diffusion barriers are required since inter layer dielectrics (ILDs), which are typically deposited at temperature above 400˚C, are present between each Cu interconnect level. Mainly, diffusion barriers must block diffusion of Cu, have low electrical resistivity, and good adhesion to Cu and to ILDs [NIC81].

A wide variety of barrier materials have been tested for Cu interconnects [WAN94, KOH09]. These materials can be categorized in: transition metals; binary metal alloys (e.g. TiW) and compounds (e.g. TaN, TiN, WN); or amorphous ternary alloys (e.g. $Ti_{34}S_{23}N_{43}$). Cu reacts with near-noble metals such as Cr, Co, Ni, Pd, and Pt in the temperature range of 250 to 450 ˚C thus these metals can be seen as sacrificial barriers (see Figure 3.8a). Sacrificial barriers are effective as long as the film is thick enough to prevent Cu diffusion and hence are of little use in IC (barrier thickness <5 nm). Metal silicides (e.g. $TiSi_2$, $CoSi_2$) fail <300 ˚C due to inter-diffusion. Cu is immiscible with refractory metals such as Mo, Ta, and W but these metals are typically polycrystalline and hence failure is caused by Cu diffusion along grain boundaries at relatively low temperatures. Binary metal alloys such as TiW are better barriers since they can be deposited by chemical vapor deposition (CVD) as amorphous films (stable up to 500˚C) and the Ti-Cu reaction is suppressed due to the presence of W. Binary metal compounds (e.g. TaN, TiN) have demonstrated good properties up to 500-600˚C and are currently extensively used. These layers are typically deposited by reactive sputtering (sputtering in N_2 ambient) or by atomic layer deposition. Barrier failure is caused by diffusion along grain boundaries. “Stuffing” of these layers during deposition to include elements that segregate at grain boundaries (see Figure 3.8b) and hinder Cu diffusion has been reported to further increase the barrier properties [KOH09].

3.2.5. Seed layer formation by sputtering/evaporation/CVD

Evaporation, sputtering, or chemical vapor deposition (CVD) deposition techniques present the advantage that a wide variety of metals can be deposited. In addition, a stack of different metals can be chosen so that each metal layer fulfills a specific requirement and can be deposited in one sequence (see Ti/Pd/Ag in section 3.2.1). These techniques are becoming attractive for the metallization of high efficiency large area cells since one can use the strong experience in the IC industry with Cu diffusion barriers and subsequent Cu electroplating.

In the method described in [MUL08], the seed layer includes three individual metal layers. The first layer should provide electrical contact to p- and n-doped regions and provide good internal reflection (e.g. Al). The second layer acts as diffusion barrier against Cu (e.g. TiW). The final seed layer (e.g. Cu) should ensure uniform nucleation for the subsequent Cu plating step. Following this, a masking layer (e.g. screen printed resist) is printed with respect to the underlying p- and n- contacts (requires alignment) and both contacts can be thickened simultaneously by Cu electroplating. Finally, the mask is removed, the seed layer is selectively etched back to isolate both polarities, and a capping layer is applied. One advantage in this process sequence is that the diffusion barrier is present everywhere between Cu and Si.

For the front side metallization (H-pattern) of solar cells, a similar plating-in-a-mask process can be applied. It is particularly suited to heterojunction (see Figure3.9a) or metal-insulator-semiconductor (MIS) solar cells. The contact/barrier/seed metal stack can be deposited directly on top of the transparent conductive oxide (TCO), which acts as an anti-reflection coating, without the need for an additional contact opening step. Therefore, no alignment is required. Since the width of the fingers is defined by the opening width in the masking layer, excellent aspect ratios have been obtained as shown in Figure 3.9b. In addition, the TCO layer has been shown to act as diffusion barrier to Cu thus deposition of the barrier metal layer might be skipped [LIU05]. However, Cu adhesion to TCO is poor and an adhesion layer is still required (typically Ni or Ti). This approach is currently followed by several groups or companies worldwide who have all shown efficiencies above 21% [HER12, MUN12, HEN13, BAL13]. Potential issues with this technique are the difficulty to define narrow openings (<20 μm) without photolithography and the cost of printing a mask covering ~95% of the wafer area.

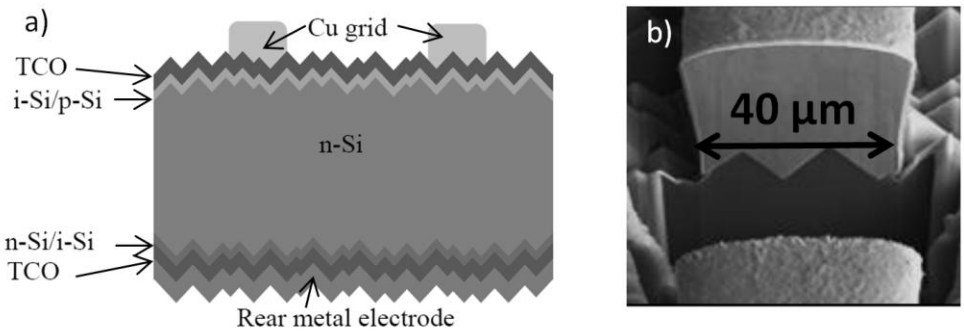


Figure 3.9: a) Example of heterojunction solar cell with a Cu front grid. taken from [HER12]. b) Cu plated finger obtained using a plating-in-mask approach. Taken from [MUN12].

Another option is to print the masking layer only where the H-pattern should remain (~5% of the area). The contact/barrier/seed metal stack can then be selectively etched, the masking layer removed and the contacts selectively Cu plated as described in [CRA12]. Unlike with the previous sequence, plating occurs in both vertical and lateral directions. Potential issues with this sequence are related to the ability to print narrow, uniform, and continuous openings.

Unlike TCO, the anti-reflection coatings (ARCs) used for Al-BSF or i-PERC type solar cells c-Si solar cells are non-conductive (e.g. PECVD SiNx:H, see Chapter 2.3). Therefore, to apply a plating-in-a-mask process an additional step is required to define openings in the ARCs which would then need to be aligned with the subsequent openings in the plating mask. As such an approach requires high alignment accuracy, self-aligned contacts are preferred.

SALICIDE or self-aligned silicides contacts are a standard process in IC industry where they are required to lower the contact resistance (see Chapter 2.2) to the gate and source/drain regions and allow higher operation speeds by reducing RC delay. Typically, metal is evaporated or sputtered and silicides are formed by rapid thermal annealing (RTA). Silicide formation does not occur at the dielectric regions separating the source/drain/gate regions (see Figure3.10a) and a subsequent selective etch removes unreacted metal leaving behind the self-aligned silicide contacts. The IC industry moved from C54-$TiSi_2$ to $CoSi_2$ and then to NiSi (see Figure 3.10b) for several reasons as the dimensions of the device kept shrinking (device scaling). Different reviews on the application of silicides in IC industry have been published [MUR95, GAM98]. A key element is that device scaling meant narrower junction depths (see Figure 3.10a) and hence silicides had to be chosen so that silicon consumption was minimized (see Figure 3.10c).

The main part of the experimental work in this thesis deals with nickel silicides as they offer low contact resistance (see Chapter 2.2), low silicon consumption (unlike cobalt silicides), and can be formed at relatively low temperatures (see Figure 3.10b). In addition, unlike Pd or Pt, Ni is an inexpensive material. Self-aligned nickel silicides using Ni layers deposited by sputtering or using electrochemical deposition methods are evaluated in details in Chapter 5.

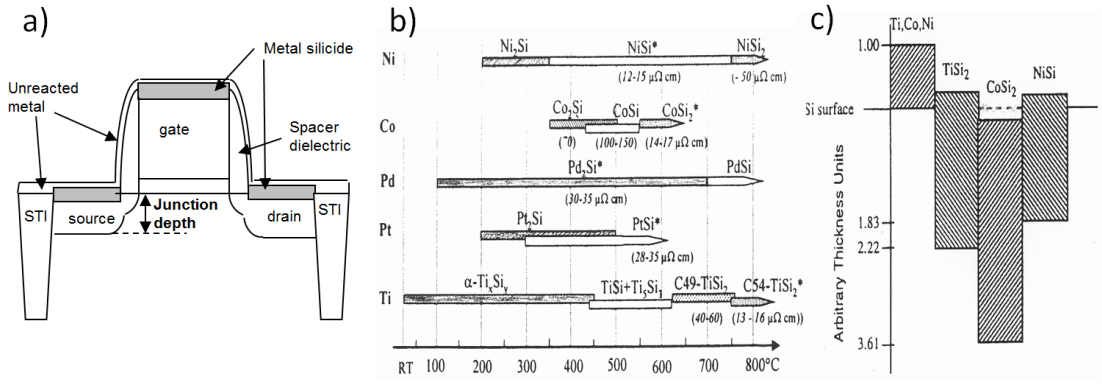


Figure 3.10: a) Schematic of a transistor with self-aligned metal silicide (SALICIDE) contacts to the gate and source/drain regions. b) Resistivity of the most common silicides versus formation temperature using rapid thermal annealing. Taken from [WOL00]. c) Silicon consumption ratios (for 1 nm of deposited metal on top, x nm is consumed in Si) of most common silicides used in IC. Taken from [WOL00].

3.2.6. Seed layer formation by laser

Seed layer metal deposition techniques as described below have not been used in this work but as they present possible alternatives they are briefly mentioned.

Laser micro-sintering (LMS) was first evaluated for the front side metallization of solar cells at Fraunhofer ISE by Aleman [ALE13]. A thin metal powder is deposited over the anti-reflective coating (ARC) and the laser beam is scanned across the surface locally sintering the metal particles. At the same time, the anti-reflective coating is opened and the metal-silicon contact is formed. The un-reacted powder is then removed and the contacts are subsequently thickened using a Ag plating step as shown in Figure 3.11a. Despite its potential, contacts formed by LMS suffered from reproducibility issues that were attributed to non-uniform powder deposits and non-uniform irradiation leading to local shunting of the emitter [ALE13].

Another approach is laser chemical metal deposition (LCMD). The wafer is immersed in the electrolyte, and a laser beam is scanned across the wafer. As the wafer surface is irradiated and heated, the ARC is opened, metal in the electrolyte is reduced, and the metal-silicon contact is formed. Although there has been some promising results by Wehkamp [WEH11], LCMD presents similar constraints as LMS since many processes are occurring simultaneously (ARC opening, metal deposition, contact sintering) leading to reproducibility issues.

A more promising approach is laser transferred contacts (LTC). In this technology, metal is first deposited on a transparent glass or foil which is brought in close proximity with the wafer. The metal layer is then transferred from the substrate to the wafer by laser irradiation. LTC have been successfully demonstrated by Roder et al. [ROD10] who was able to form 7 μm wide Ni contacts which were then Cu plated as shown in. The contact formation between Ni and silicon was already achieved during the LTC. However, adhesion and long-term reliability results of contacts formed by LTC have yet to be demonstrated.

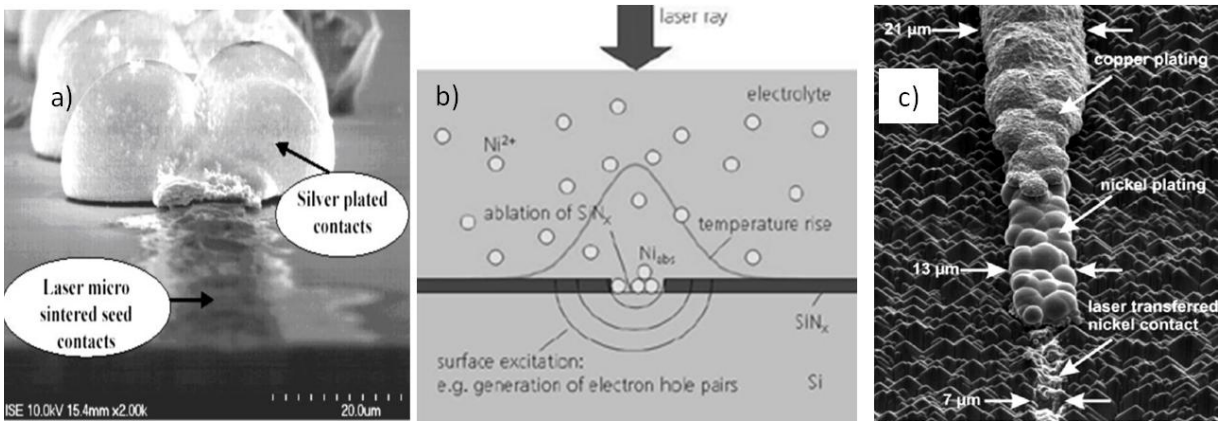


Figure 3.11: a) Ag plated finger with seed layer formed by laser micro-sintering (LMS). Taken from [ALE13]. a) Schematic of laser chemical metal deposition (LCMD). Taken from [WEH11]. c) Contact formation steps from bottom to top: laser transferred nickel contact, nickel plating, and Cu plating. Taken from [ROD10].

3.2.7. Seed layer formation using electrochemical deposition

As it was mentioned in section 3.2.5, self-aligned nickel silicides are interesting for the front side metallization of silicon solar cells because they offer low contact resistance to lowly doped emitters, can be formed at low temperatures, and because Ni is rather an inexpensive material (compare to Pt and Pd). We also mentioned in section 3.2.4 that, based on experienced in the IC industry with barriers against Cu diffusion, nickel silicides and nickel can be regarded as sacrificial barriers against Cu diffusion. Therefore, techniques enabling the deposition of relatively thick layers might be beneficial. This is the case with electrochemical deposition which present the advantages of being relatively simple, efficient (self-aligned layers hence no material waste like with sputtering/evaporation), and fast. One distinguishes between electroless plating, electrolytic plating, and immersion plating. In electroless plating, deposition is achieved using a reducing agent present in the electrolyte which provides the electrons to reduce metal ions at the silicon surface. In electrolytic plating, the source of electrons can be provided by an applied external potential or by the light-induced current of a solar cell. In immersion plating, no reducing agent is present, the substrate is the source of electron for the deposition and the process is self-terminating (only thin layers can be formed). Historical developments of nickel deposition using electroless and electrolytic methods are given below. Both have been evaluated extensively in this thesis in a seed-and-plate approach using Cu plating, thus the working principle and impact of process parameters are discussed in Chapter 5. Nickel seed layer deposition by immersion plating has only been demonstrated very recently [YAO13] and was not evaluated in this thesis.

3.2.7.1. Electroless deposition

In the early 1980s, Motorola established a process for terrestrial solar cells based on photolithography patterning and Ni/Cu metallization [GAL86]. Motorola selected electroless Ni because solar cells for space applications had already been made with this process [SUL57]. At first, an initial electroless Pd deposition step followed by a sintering step to create palladium silicide (Pd_2Si) was performed prior to electroless Ni. This was required to achieve good ohmic contact and good adhesion [COL80]. Motorola was later responsible for forming the silicide directly with Ni (Ni_2Si) thus dropping out the expensive initial Pd deposition step. In this case, the optimized contact architecture: Ni_2Si/Ni was used as sacrificial barrier against Cu diffusion and was shown to meet the required criteria (no power degradation at 250˚C for 1h) [GRE81b].

In 1984, Green and Wenham [GRE84] patented a concept called laser grooved buried contact (LGBC) cell. Photolithography patterning was replaced by laser-scribed grooved contacts and electroless plating was used to fill the grooves as shown in Figure 3.12. The main advantage of the LGBC technology is that since the contacts are “buried” very high aspect ratios (width around 20-40 μm and depth around 60-100 μm) can be obtained thus minimizing fill factor and shading losses. In addition, the use of a selective emitter enables the combination of a

lowly doped (n^+) surface in between the contacts (improves Voc potential and collection efficiency in short wavelength) and a heavy doping (n^{++}) under the contacts (reduces recombination and contact resistance losses) [GRE84]. The original LGBC process relied on high temperature steps: (i) $POCL_3$ diffusion at ~800˚C to form a shallow ~150 Ω/sq n^+ emitter, (ii) thermal oxidation at >1000˚C to form a thick SiO_2 layer, and (iii) a heavy $POCl_3$ diffusion at ~950˚C leading to ~5 Ω/sq n^{++} in the grooves and enabling Al p^+ BSF formation at the rear [RIC04]. Hereafter, the front metal grid underwent a series of wet processing steps using the thick SiO_2 layer as a plating mask (see Figure 3.12b). After HF deglazing (native oxide removal in the grooves), a layer of electroless Ni (~100 nm) was deposited in the grooves and sintered at ~400 ˚C in N_2 to form nickel silicide contacts. After sintering, excess Ni was removed in HNO_3, the surface re-activated by a short HF dip, a second Ni layer (~100 nm) deposited prior to electroless Cu deposition (~5 µm), and the contacts were capped with a thin Ag layer to improve solderability [JEN03]. Finally, the SiO_2 layer was etched back to a thickness of around 100 nm.

The LGBC process was licensed to several companies. Most notably, BP Solar who commercialized LGBC cells in the years 1992-2008 used low pressure chemical vapor deposition (LPCVD) of silicon nitride Si_3N_4 as diffusion/plating mask instead of the thick thermal oxide [BRU03, JEN03]. Such nitrides are denser thus are ideal to prevent parasitic plating but do not provide good surface passivation [RIC04]. Early modules fabricated by BP Solar with LGBC cells are still in operation today thus demonstrating long-term reliability in the field of this cell architecture. Several other dielectrics layers meeting the diffusion/plating mask and anti-reflection coating requirements were also evaluated and results can be found in [RIC04]. Efforts were also made, in the so-called simplified buried contact (SBC) technology [WEN96], to use screen-printing Al (and firing) at the rear and an homogeneous emitter at the front thereby eliminating two high temperatures steps. Since the LGBC process was mainly limited by the recombination at the rear, electroless Ni/Cu deposition was also used for more advanced buried-contacts cell concepts. These include double-sided LGBC cell and interdigitated backside buried-contact cell [GUO05] as well as LGBC with laser-fired-contacts at the rear where efficiencies up to 20.1% were demonstrated on large area [MAS06, SHU06].

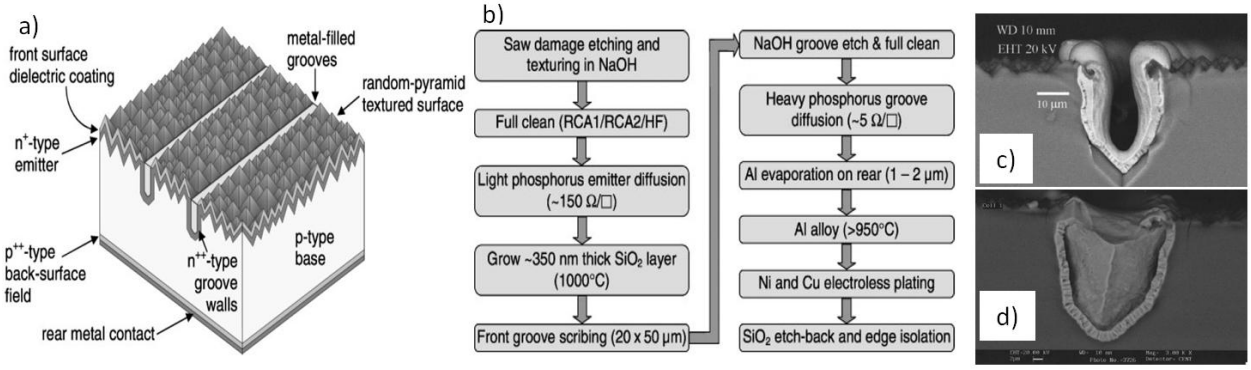


Figure 3.12: (a) Schematic of laser grooved buried contact (LGBC) cell and (b) standard LGBC sequence using thermal SiO2 as diffusion/plating mask, taken from [RIC04]. Scanning electron microscope image of (c) LGBC contact filled by electroless of Ni/Cu and (d) filled by electroless Ni and electroplating of Cu, taken from [JEN03].

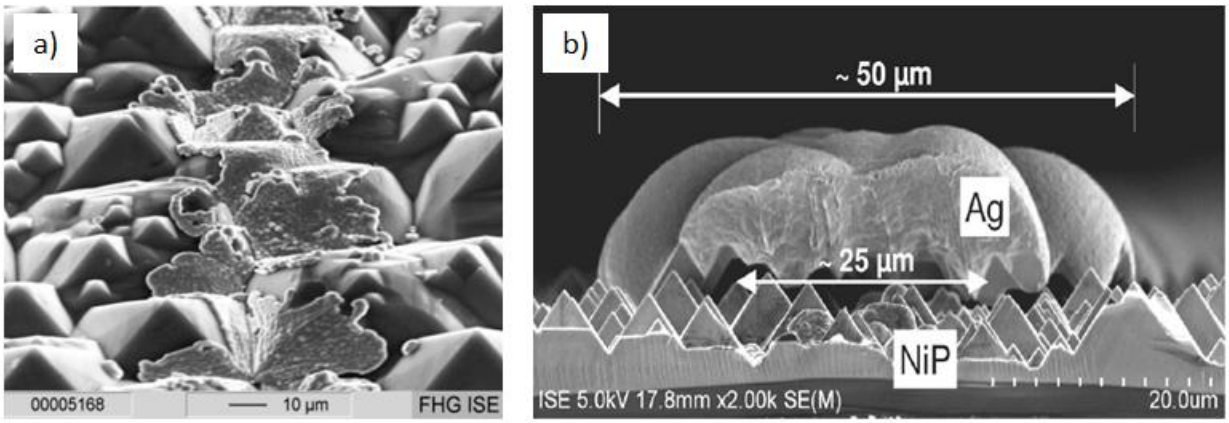


Figure 3.13: (a) Scanning electron microscope (SEM) image of electroless Ni layer in a laser ablated finger taken from [ALE13]. (b) SEM image of Ag plated finger using (a) as seed layer. From [ALE13].

To enable further process simplification, alternative front dielectric(s) patterning techniques to the laser-grooved contacts that would eliminate the laser damage etch and groove diffusion steps have been the focus of intense research in recent years. Techniques currently under investigation include laser ablation and laser-doped selective emitters (LDSE) since they enable direct removal of the front dielectric(s), ultra-fine line (down to ~10 µm wide), and can offer short processing time (few seconds per wafer). However, they present several challenges. One challenge is to selectively remove the dielectric(s) without damaging the underlying p-n junction as the diffusion of Ni during nickel silicide formation along locally defected areas might create recombination paths thereby strongly reducing the pseudo fill factor (see Chapter 2.1.3). In addition, such laser defects might compromise long-term reliability and hence the diffusion barrier developed by BP Solar (thin NiSi/Ni) might have to be revisited. Finally, as the contacts are no longer buried in Si, the contact area is greatly reduced (compare Figure3.13 to Figure3.12b) which might increase contact resistance losses and affect mechanical adhesion.

As experienced by BP Solar, industrial implementation of electroless deposition is not without problems. Typically, electroless deposition rates are rather slow (~100 nm/min) and hence wafers need to be processed in large batches to achieve sufficient throughputs. In addition, electroless baths typically require careful monitoring (pH, temperature, concentration of reducing agent) and need to be periodically replaced since they are prone to extraneous plating (plating occurring on particles, tank walls) and decomposition. Therefore, electrolytic plating baths, which by definition do not contain any reducing agents, are more beneficial. In addition, they also enable faster plating rates and hence are particularly favorable for the deposition of Cu or Ag since thick layers (5-15 µm) are required.

3.2.7.2. Electrolytic deposition

For electrolytic deposition, one distinguishes between electroplating and light-induced plating (LIP). Electroplating offers the highest degree of control and the fastest plating rates (up to several µm/min) since the source of electrons is directly controlled by an external power supply. However, electroplating requires a seed layer with a certain conductivity to minimize the potential drop with increasing distance from the contact point(s) and achieve uniform deposits. On the other hand, LIP enables direct plating of metal on Si with relatively fast plating rates (up to ~ 1 µm/min). LIP presents the advantage that the front side can have a uniform potential under illumination thus enabling homogeneous plating. LIP can either be performed contactless ("non-contact LIP") or simply by contacting the rear side of the cell ("bias-assisted LIP"). The working principles of both non-contact LIP and bias-assisted LIP are presented in Chapter 5.

Historically, LIP has been mainly used for silver plating in high efficiency cells as it constitutes a fast method to thicken contacts in a seed-and-plate approach. In order to reduce waste management costs, considerable efforts have been put in achieving comparable results with cyanide-free Ag plating solutions [HOR09a] and gaining fundamental understanding of light-induced silver plating [MET07, BAR12]. As the results were promising (see Chapter 3.2.3) and owing to relative simplicity of the LIP process, a number of LIP toolsets (example in Figure3.14) are either commercially available today or under development [RIC13].

The use of light-induced plating for nickel seed layer deposition is very recent and coincides with the on-going development of cell architectures with non-grooved contacts (see Figure 3.14c). Recent investigations using laser-doping for the front dielectric(s) patterning performed indicate that nickel seed layers deposited by LIP perform better than their counterparts deposited by electroless [HAM11]. However, contact adhesion and long-term reliability are tasks that need to be addressed. Also, currently the sintering step to form nickel silicide is performed directly after the deposition of the nickel seed layer (electroless Ni or LIP Ni). It would be advantageous to sinter at the end of the plating process (Cu + capping layer) since all layers can be deposited in one sequence using one plating toolset.

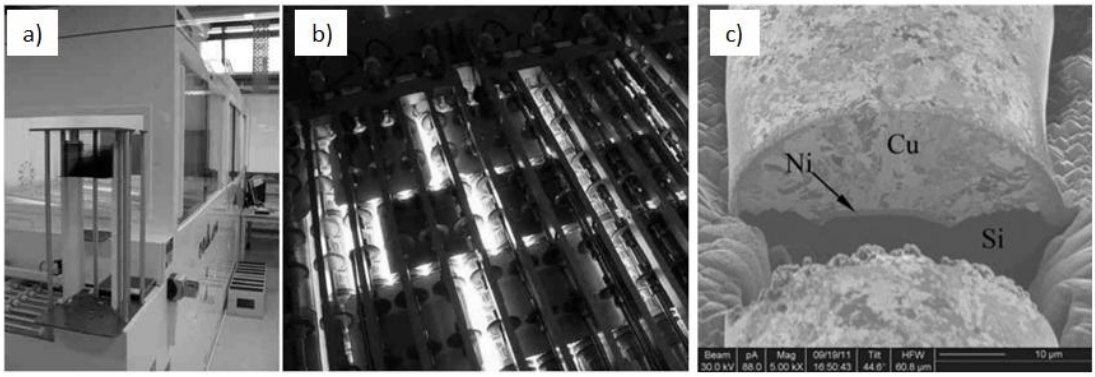


Figure 3.14: (a) Inline light-induced-plating (LIP) machine developed by Fraunhofer ISE and Gebr. Schmid. (b) Wafers during LIP plating, wafers are contacted at the rear (top side) by rollers. Taken from [BAR12] (c) Scanning electron microscope image of Ni/Cu finger obtained by LIP. Taken from [LEN12].

3.3. Competing metallization concepts at module level

The metallization concepts described here have in common that they eliminate the need for busbars and that they help reducing losses both at cell level and module level.

The first concept is the Day4^{TM} Electrode concept [SCH06]. It consists of a mesh of 10 to 20 copper wires to interconnect the cells instead of using tinned (typically Sn/Ag/Pb) copper tabs soldered on the busbars (see Figure3.15a). The copper wires are coated with a metal with a low melting point (Sn-In) and connections to the fingers is achieved during lamination (T<200˚C). Since the current increases linear and the power loss to the square with finger length, a high conductivity of the finger is necessary which requires a large cross section area of the finger. By adding more busbars, the unit finger length (maximum distance the current travels to reach a busbar) can be lowered. This reduces shading losses, electrical losses, and Ag consumption.

Numerical simulations were performed by Mette [MET07] who compared 3 busbars designs to a mesh of 16 wires in a seed-and-plate approach (Ag plating). He calculated that a total power loss of less than 5% can be achieved with the mesh of 16 wires for optimum contact width compared to 7.2% with 3 busbars. He also calculated that the required silver thickness is between 2 and 4 µm which corresponds to 20 to 40 mg of Ag as compared to 152 mg with 3 busbars. Such low Ag consumption falls in line with the ITRPV requirements for beyond 2017 (compare section 3.1.3) and do not require the use of Cu contacts. Meyer Burger acquired a license for the Day4^{TM} Electrode concept and intends to commercialize it under the name of Smart Wire Contacting Technology (SWCT) [PAP13]. A similar approach is also under development at Gebr. Schmid under the name "multi-busbars" where copper wires, as shown in Figure3.15b, are simultaneously soldered prior to lamination [BRA13]. Improvements at module level have been demonstrated with both approaches [PAP13, BRA13] and reliability testing are on-going [PAP13]. Potential challenges include measuring and sorting cells with fingers only, demonstrating the robustness of the process, and demonstrating the overall cost advantage particularly for the SWCT due to the costs associated with the use of Sn-In coating [PAP13].

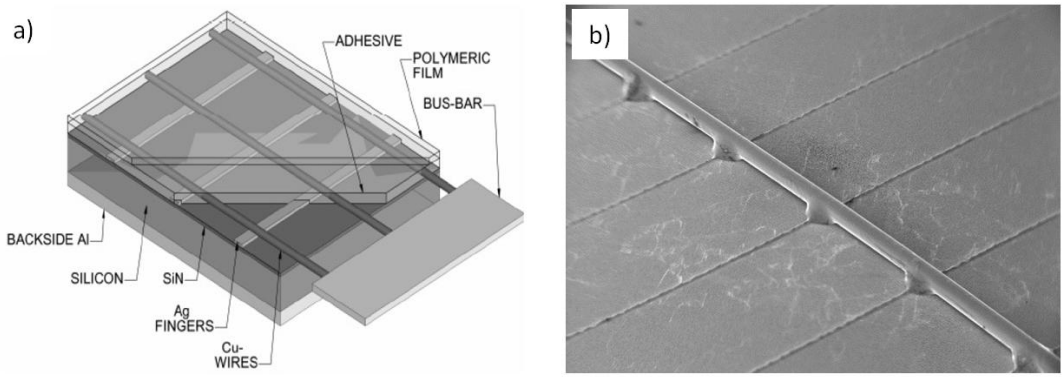


Figure 3.15: (a) Solar cell with Day4TM Electrode concept: copper wires with low melting point metal coating are embedded in polymeric film/adhesive. The coating melts upon lamination enabling robust contact with cell fingers. [SCH06] (b) Scanning-electron microscope image of "multi-busbars" concept from Gebr. Schmid showing one Cu wire soldered to Ag fingers. Soldering is performed prior to lamination. Taken from [BRA13].

A second concept is to use electrically conductive adhesives (ECA) to connect fingers to the tinned (typically Sn/Ag/Pb) copper tabs. Typically ECA contain metal particles dispersed in an adhesive resin and require combined pressure and heat to become conductive. ECA present numerous advantages. Typically, the bonding process eliminates the need for flux and is typically done at lower temperatures than with standard soldering (~230˚C for Pb-containing tabs and ~260˚C Pb-free tabs) which minimizes thermal stress applied to the wafer. Again, busbars are not required which eliminates the recombination losses under the busbars and drastically reduce Ag consumption. Unlike with conventional spot soldering, ECA are connected along their entire length to the ribbons and hence eliminate the losses caused by the busbar resistance. In addition, since the resins offer some degree of movement they can better withstand the stress imparted by thicker tabs. Using thicker tabs is beneficial as either the losses due to tab resistance can be reduced either fewer busbars can be used thereby reducing shading losses. Finally, ECA also enable the use of grooved tabs as shown in Figure3.16 which once encapsulated can reflect part of the light back into the cell thus reducing the effective shading area at module level. Potential challenges include demonstrating: i) the cost advantage of ECA at module level, ii) long-term reliability, and iii) tabber-stringers for ECA with sufficient throughputs.

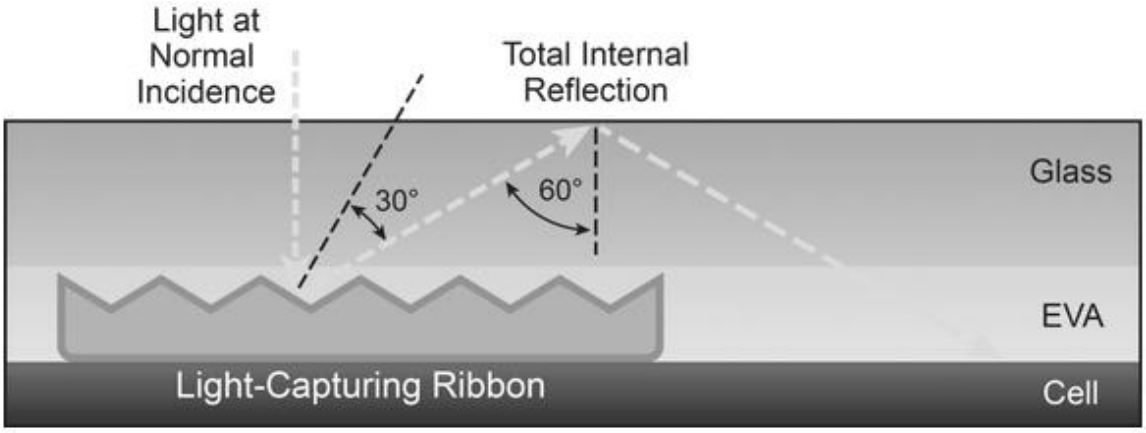


Figure 3.16: Schematic of silver plated light-capturing ribbon (LCR) from Ulbrich solar technologies.

3.4. Approach and challenges

In this chapter, we explained that the co-optimization of screen design, printing parameters, and printing pastes has been key to push the limits of industrial screen printing of Ag for the front metallization of silicon solar cells. However, despite these improvements screen printing (SP) of Ag presents intrinsic limitations which are:

- Ag represents around 1/3 of total cell processing costs (February 2013)
- Ag production is limited and industrial demand is likely to rise
- SP and fired Ag contacts are currently limited to non-optimum phosphorous emitters with surface concentrations ~$1x10^{20}$ cm^{-3}
- SP imparts mechanical stress to wafers which might result in wafer breakage
- State-of-the-art screens for fine-line printing are more expensive, are more fragile, and are more likely to lead to finger interruptions
- Contact widths below 30 μm are difficult to achieve in a reproducible manner even with fine-line printing techniques.

The PV industry acknowledges that the reduction of Ag below 50 mg/cell by 2017 is a mandatory step to reduce production costs. In addition, energy conversion efficiencies beyond 20% on p-type and beyond 21% on n-type for large area silicon solar cells are expected in production by 2017.

To overcome the limitations of screen-printing of silver, a seed-and-plate approach is thought to be the most appropriate as it enables the separate optimization of the contact properties and the lateral conductivity. Numerous seed-and-plate technologies have been demonstrated based on fine-line printing of silver pastes or inks followed by Ag plating. However, these technologies do not solve the contact resistance limitations of Ag pastes/inks nor enable a drastic reduction of Ag consumption.

The use of self-aligned nickel/copper (Ni/Cu) plated contacts seems to be the more viable option for the front side metallization of homo-junction silicon solar cells. Based on the experience in the IC industry and with early solar cells for space applications, the use of Ni to form nickel silicides contacts upon sintering is the most promising approach. Nickel silicides offer low contact resistance, low silicon consumption (unlike cobalt silicides), and can be formed at relatively low temperatures. In addition, unlike Pd or Pt, Ni is an inexpensive material and, unlike Ti, can be deposited using electrochemical methods. Cu is the second most conductive metal after silver and hence is ideally suited to replace Ag. Finally, nickel silicides contacts have been shown to be sufficient as sacrificial barrier against Cu diffusion in early solar cell devices produced by Motorola and by BP Solar.

Self-aligned nickel silicides contacts can be formed using nickel deposited either by sputtering/evaporation, electroless, or electrolytic methods. In order to use a simple and cost-effective process, current solar cell developments are directed towards alternative front dielectric(s) patterning techniques than the laser-grooved contacts used by BP solar. However,

alternative front dielectric(s) patterning techniques such as laser-ablation or laser-doping are quite challenging and need to be optimized. Finally, the nickel silicide sintering step can be performed either prior to Cu plating or afterwards which would be preferred as it enables to deposit all metal layers in one sequence.

It is the objective of this thesis to demonstrate a simple and reliable process for the formation of Ni/Cu plated contacts for the front side metallization of high efficiency industrial silicon solar cells. This requires the evaluation of different nickel deposition techniques. In addition, the interactions between emitter profile, front dielectric properties, dielectric patterning techniques, nickel silicide formation, adhesion, and long-term reliability need to addressed. Also, the process need to be transferred to pilot production tools. Finally, the cost and efficiency advantages over screen printing of Ag need to be demonstrated. This last point is particularly challenging as not only enormous progress have been made in recent years with screen printing of Ag but there is also competing metallization concepts at module level that enable drastic reduction of Ag consumption and improved efficiencies. Finally, to illustrate the "fast-moving target" that is screen-printing of Ag, selected best large area results of p-type mono-crystalline silicon solar cells are given in Table 3.1.

Table 3.1: Selected best large area p-type mono-crystalline silicon solar cells fabricated until early 2013.

cell type	pattern ARC	front metal	Size	Voc	jsc	FF	eta	Reference
			[mm]	[mV]	[mA/cm^2]	[%]	[%]	
AL-BSF	-	SP Ag	125	625	36	80.2	18.0*	[MET07]
AL-BSF	-	SP Ag	156	640	37.9	78.4	19	[HAH10]
AL-BSF	-	SP Ag	156	649	38.8	79.1	19.9*	[MET13]
AL-BSF	LGBC	ELESS Ni/Cu	125	625	36.3	80.6	18.3*	[MAS04]
AL-BSF	LDSE	LIP Ni/Cu	125	638	38.4	78.8	19.3*	[HAL11]
AL-BSF	LDSE	LIP Ni/Cu	156	642	38.8	79.6	19.8*	[KYE12]
LBSF	-	SP Ag	125	632	34.6	75.3	16.5	[AGO05]
LBSF		SP Ag + LIP Ag	156	652	38.9	79.9	20.2*	[MOH11]
LBSF	-	SP Ag	156	664	39.9	79.2	21.0*	[MET13]
LFC	LGBC	ELESS Ni/Cu	125	674	37.9	78.7	20.1	[MAS06]
PERL	LDSE	LIP Ni/Cu	156	665	40.9	74.4	20.3*	[WAN12]
LBSF	laser	LIP Ni/Cu	156	665	39.9	80.5	21.3*	[MET13]

*Confirmed at ISE Callab

Al-BSF: full Al Back Surface Field, LBSF: local Al BSF, LFC: Laser Fired rear Contacts,

PERL: Passivated Emitter and Rear Locally diffused (=local boron BSF),

LGBC: Laser Grooved Buried Contact, LDSE: Laser Doped Selective Emitter

SP Ag: Screen Printed and fired Ag contacts, ELESS: Electroless, LIP: Light-Induced Plating

CHAPTER 4

Front side design

In this chapter, basic simulations are performed to evaluate the impact of front emitter design and front metal grid design. Based on these simulations we define the electrical requirements of self-aligned nickel/copper plated contacts for the front side metallization of industrial high efficiency silicon solar cells.

4.1. Front emitter design

There are numerous techniques to form the phosphorous-doped front-side emitter in p-type silicon solar cells and the resulting dopant profile plays an important role in achieving high efficiency devices. The optimization of the dopant profile should not be performed independently from the front metal grid design as factors such as surface and bulk emitter recombination, grid shading, and series resistance are competing. The use of double-diffused or selective emitters resolves many of the trade-offs and hence offers higher efficiency potential [SAN09]. Numerous techniques for the formation of selective emitters have been evaluated for production [HAH10]. We only discuss here the impact of homogeneous emitter design not only because homogeneous emitters are simpler to fabricate but also because they are able to provide a sufficient efficiency level in many cases.

In industry, the front-side emitter is typically created by phosphorous in-diffusion from a gas source (batch $POCl_3$ diffusion) or from a liquid source (inline diffusion) that can be spin-on or spray-on [SZL06, BEN06]. $POCl_3$ diffusion or inline diffusion are generally performed at temperatures in the range of 750 to 900˚C leading to emitter profiles with a high phosphorous concentration close to the surface (N_s>1x10^{20} at/cm^3) which is required to achieve low contact resistance values with screen printed silver contacts [BEA12]. However, such emitters often present a "dead-layer" close to the surface as the phosphorous concentration exceeds the solid solubility of phosphorous in Si (~2x10^{20} at/cm^3) [BEN06, HOR10b] (see Figure 4.1a). In the recent years, several approaches to reduce the dead-layer have been investigated as this lowers bulk emitter recombination and hence improves the short wavelength response ("blue-response") of the device. Examples of successful approaches include optimizing the $POCl_3$ diffusion parameters [CHO05, SHI13], removing the source of dopants after diffusion and performing a low temperature oxidation [BIR09, PRA12], or chemically etching away the dead-layer [HAV08, LAC12]. Nowadays, implantation in combination with thermal oxidation to active dopants is being evaluated as an alternative technique for the formation of phosphorous doped emitters [ROH10]. Compared to in-diffusion techniques, implantation offers improved sheet resistance uniformity which is beneficial to achieve tight efficiency distributions [DUB11].

In high-efficiency devices (laboratory cells with Ti/Pd/Ag evaporated contacts, Ni/Cu plated contacts), the front-side emitter is not limited to surface concentrations above $1x10^{20}$ at/cm^3 thanks to the excellent contact properties of Ti or Ni. This enables the use of optimum emitters which have sheet resistance values in the range of 100 to 150 Ω/sq, present a low surface concentration (N_s~$1x10^{19}$ at/cm^3), and are relatively thick (~1-2 µm) to reduce surface recombination under the contacts [CUE00, SAN09].

To better understand the influence of front emitter design on the efficiency of i-PERC solar cells, we carried out PC1D simulations [BAS88] for various emitters. These included an industrial emitter typically used with screen printed Ag contacts (R_{sh}~85 Ω/sq), a shallow emitter which cannot be contacted by screen printing of Ag (R_{sh}~150 Ω/sq), and a high-efficiency deep emitter (R_{sh}~130 Ω/sq). SIMS profiles (chemical phosphorous concentration), given in Figure 4.1a, were used as inputs expect for the 85 Ω/sq emitter for which we used the SRP profile (electrically active phosphorous concentration). The electrical and optical parameters that were assumed for the PC1D simulations are given in Table 4.1. The effective rear-surface recombination velocity (RSRV) and the internal reflectance values are typical for i-PERC solar cells in this work. The external front reflectance, accounting for both busbar and fingers shading (total shading ~5%), was taken from experimental data for a cell featuring a similar 130 Ω/sq deep emitter and Ni/Cu plated contacts. External front reflectance and internal reflectance parameters were assumed to be identical for all emitters. PC1D simulations were performed for each emitter for a range of effective front surface recombination velocity values (FSRV) which account for recombination at the front passivated surfaces as well as in the emitter bulk (e.g. inactive dopants in the top-most emitter region causing additional SRH recombination).

Table 4.1: Assumed parameters for the PC1D simulations of i-PERC solar cells given in Figure 4.1b.

Assumed parameters	value	unit
Device area	1	cm^2
Front surface texture depth	5	µm
Front reflectance	measured data	
Internal reflectance:		
front first bounce	94	%
front subsequent bounce	94	%
rear first bounce	94	%
rear subsequent bounce	92	%
Emitter + base contact	0.5	Ω
j_{02} recombination (n=2)	$5x10^{-9}$	A/cm^2
Internal shunt	$1x10^4$	Ω
Thickness	160	µm
Intrinsic carrier concentration (at 300K) [WOL10].	$9.65x10^9$	cm^{-3}
Base doping	$1x10^{16}$	cm^{-3}
Bulk recombination	1500	µs
Effective rear-surface recombination velocity (RSRV)	70	cm/s

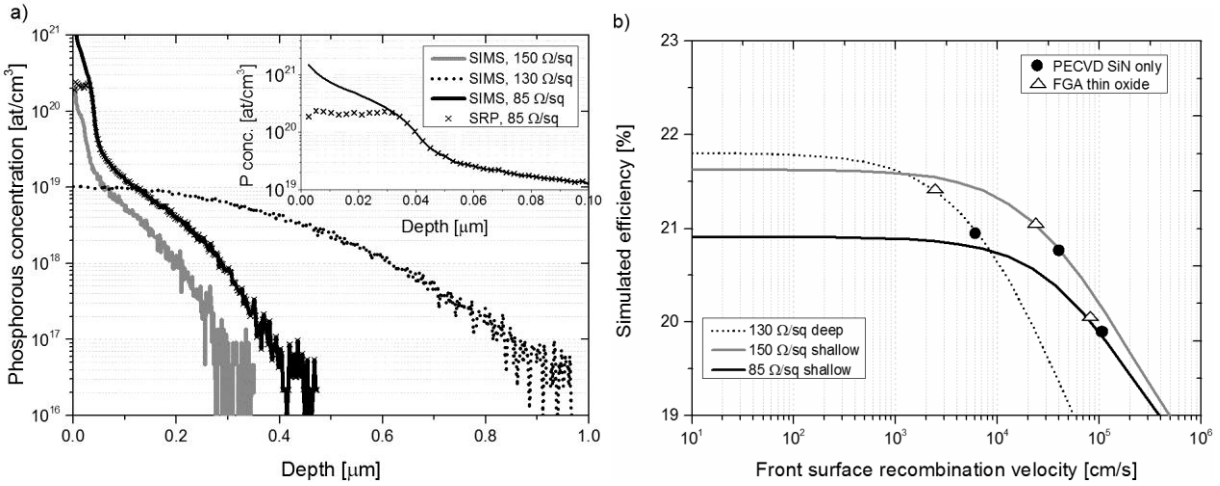


Figure 4.1: a) SIMS measurements of three different phosphorous emitters b) PC1D simulated efficiencies for the emitters given in (a) as a function of the effective front surface recombination velocity. Symbols are taken from the data from Kerr given in Fig. 4.2 and multiplied by a factor 4 to account for the front textured surface.

The PC1D simulation results given in Figure 4.1b indicate that the 130 Ω/sq deep emitter yields the highest efficiency potential provided FSRV values below $1x10^4$ cm/s can be achieved. This is because both the 85 Ω/sq emitter and the shallow 150 Ω/sq emitter are limited by Auger recombination which increases with surface doping level.

Fundamentally, a reduction of surface recombination can be achieved by: i) reducing the density of interface traps (D_{it}) and ii) minimizing the concentration of minority carriers at the surface by field effect passivation (see Chapter 2.1.3). In practice, achievable FSRV values for phosphorous doped emitters strongly depend on surface doping concentration, the chosen surface passivation scheme, and surface morphology [ALT00, KER02, GLU05]. As evidenced by the work of Kerr on planar <100> FZ-Si [KER02], thermally grown silicon oxide layers yield lower surface recombination velocity values than silicon nitride layers deposited by plasma enhanced chemical vapor deposition (PECVD) thanks to lower D_{it} values. In addition, the passivation properties of the silicon oxide layer can be improved by a post-treatment to increase the H_2 level at the Si-SiO_2 interface (see Figure 4.2a) which further reduces D_{it}. Examples of post-treatments include high temperature firing (>600 ˚C) of a PECVD a-SiN_x:H layer on top of SiO_2, forming gas annealing (FGA, H_2/N_2 mixture, ~400 ˚C), or performing an alneal treatment. The alneal treatment consists of sintering (~400 ˚C) an aluminum layer evaporated on top of SiO_2 and etching the aluminum away after sintering [ZHA96]. FSRV values on textured surfaces are typically found a factor 3 to 5 higher than on planar surfaces since textured surfaces result in higher D_{it} and suffer from non-uniform doping effects [GLU05]. This effect was accounted for in Figure 4.1b where (● and Δ) symbols represent achievable FSRV values for PECVD SiN and SiO_2+ FGA respectively based on the known emitter N_s values and Kerr's data multiplied by a factor 4. The 150 Ω/sq shallow emitter seems to be the most promising emitter because it can potentially bring efficiencies closed to the ones achievable with the 130 Ω/sq deep emitter while being simpler to manufacture since a long high-temperature drive-in step is no longer required.

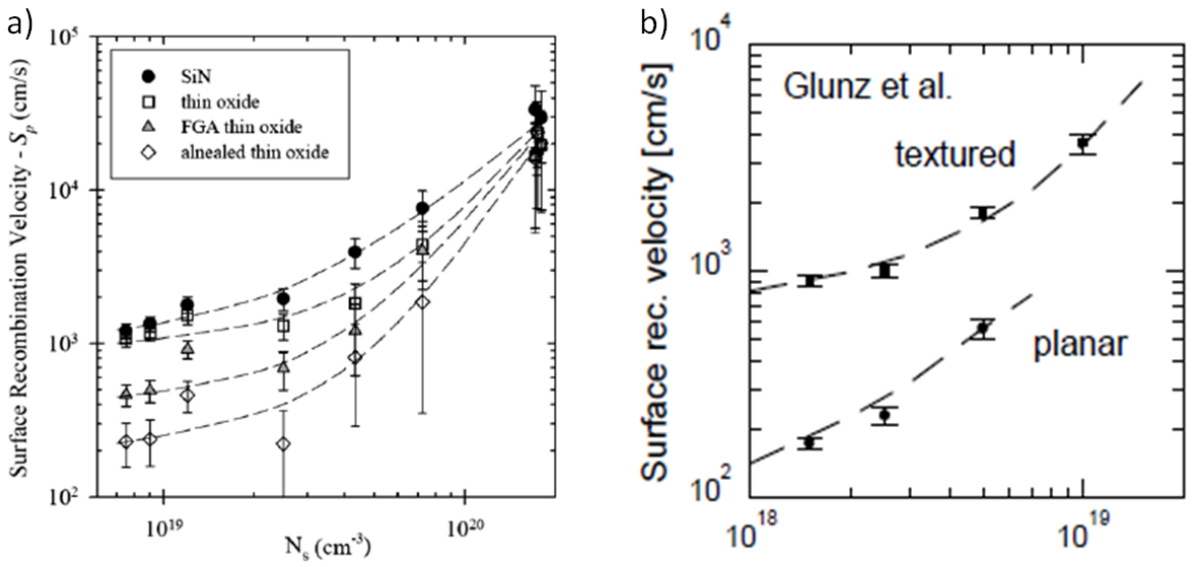


Figure 4.2: a) Surface recombination velocity for different passivation schemes as a function of surface phosphorous doping concentration on planar <100> FZ-Si [KER02] b) Surface recombination velocity versus surface phosphorous doping concentration on textured and planar silicon [ALT00].

The PC1D simulations performed so far did not include the impact of recombination at the metal-contact surfaces and the impact of emitter depth on j_{02} recombination. Recombination at the metal-contact surfaces strongly increases for lower surface doping concentrations and for lower emitter depths [SAN09]. An increase in j_{02} recombination can have an extremely detrimental effect on the fill factor and the resulting power output of the device.

To illustrate the impact of recombination in the space charge region (j_{02} recombination), we calculated, using the two-diode equation given in equation (2.4), the achievable fill factor as a function of j_{02} for various j_{01} values. We assumed a photo-generated current of j_{ph}=39.5 mA/cm^2, a shunt resistance r_p=1x10^4 Ω.cm^2, and performed the calculations for r_s =0 and r_s=0.5 Ω.cm^2 which is a typical r_s value for a good i-PERC device. From the results, given in Figure 4.3, j_{02} values should be kept below 5x10^9 A/cm^2, particularly for high-efficiency devices with excellent j_{01} values, in order to achieve fill factors above 80%.

Achieving low j_{02} values is strongly dependent on the metallization sequence and the emitter depth. As a result, the 130 Ω/sq 1 μm deep emitter will be inherently more robust than a 150 Ω/sq 0.3 μm shallow emitter. In the case of self-aligned nickel/copper contacts, achieving low j_{02} values requires: i) developing patterning techniques for the front dielectric that do not create extended damage to the emitter, ii) controlling nickel silicide formation, and iii) ensuring long-term reliability to prevent nickel or copper to diffuse to the space charge region during the lifetime of the module. Therefore, it is an objective of this thesis to co-optimize the nickel/copper metallization sequence and the emitter profile shape to enable reliable, high efficiency, and cost-effective solar cell devices.

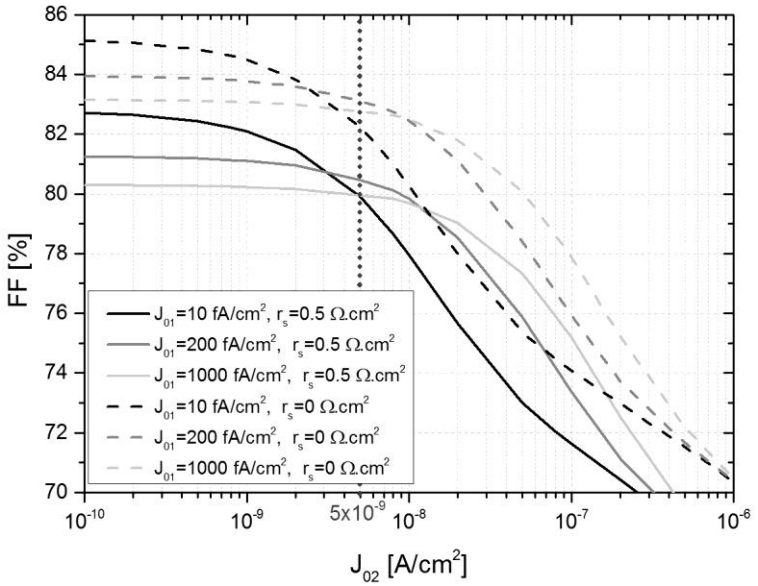


Figure 4.3: Impact of j_{02} on fill factor for different j_{01} and r_s values.

4.2. Front metal grid design

4.2.1. Analytical model and assumptions

An optimization of the front metal grid design to minimize series resistance and optical power losses for a two-layer contact structure has already been performed by A. Mette in his PhD thesis [MET07]. In this section, we implemented the individual series resistance and optical contributions of the front metal grid calculated by Mette in the two-diode equation and optimized the grid design to maximize the power output. This approach presents the advantage of including the effect of the front grid design on open-circuit voltage losses. Recombination losses under the front contacts should also impact the short circuit current density. However, this is difficult to implement in a simple analytical model. This effect was not included in the present calculations.

In i-PERC devices, the dark saturation current density for the bulk and rear surface j_{0b} is relatively low since the bulk lifetime is high and the rear surface is well passivated. Consequently, the recombination under the front contacts $j_{0e,met}$ gains in importance particularly if the dark saturation current density in the passivated areas between the contacts $j_{0e,pass}$ is low which is the case for a high-efficiency homogeneous emitter. The effect of the contacted area fraction p_{cont} on the dark saturation current density j_{01} can be calculated by:

$$j_{01} = j_{0e} + j_{0b} = j_{0e,pass} \cdot (1 - p_{cont}) + j_{0e,met} \cdot p_{cont} + j_{0b} \quad (4.1)$$

The series resistance losses will be lower if the contact area increases. However, this will also lead to increased open-circuit voltage losses and increased shading losses. Shading losses are affected by grid design and contact geometry. In the case of nickel/copper plated contacts, a thin nickel layer (typically < 2 µm) is isotropically thickened by copper plating. This means that if the initial contact width is w_c and the plated height is h_f, the final finger width w_f will be:

$$w_f = w_c + 2 \cdot h_f \quad (4.2)$$

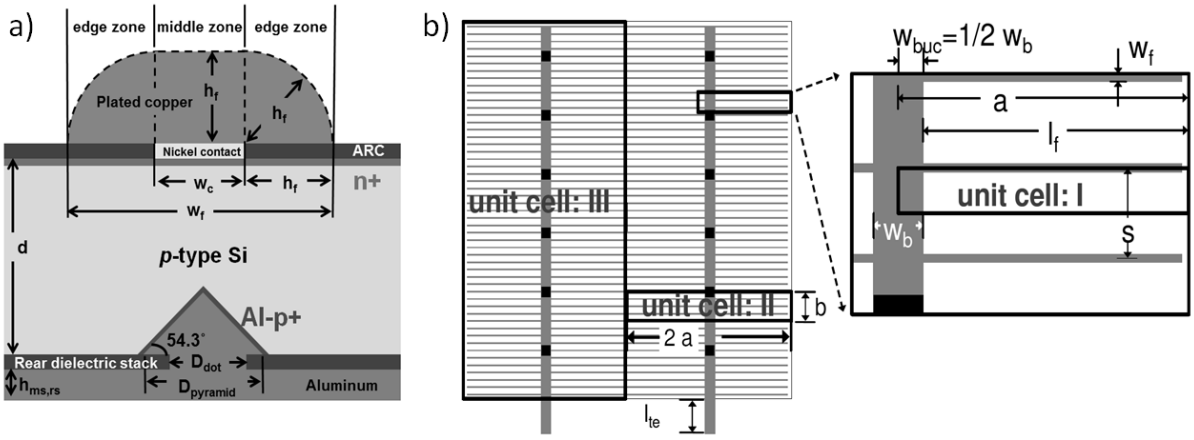


Figure 4.4: a) Schematic of i-PERC solar cell with nickel/copper plated contacts. b) Schematic of H-grid front metallization pattern illustrating the unit cells I, II, and III used for resistance calculations in Table 4.2 [MET07].

In addition, since the plated contacts are typically flat in the center and roundish at the edges (see Figure 4.4a), the cross-section area of the plated finger can be calculated by:

$$A_f = w_c \cdot h_f + \frac{1}{2} \cdot \pi \cdot \left(h_f \right)^2 \tag{4.3}$$

The total shading fraction is dependent on the finger spacing s and a which is the length of the unit cell I shown in Figure 4.1b. In addition, due to their shape, semi-roundish contacts can reflect some of the incident light back into the cell. This effect can become even more important after encapsulating the cell into the module since multiple reflections can occur between the contacts and the glass. Calculations performed by Blakers [BLA92] suggest that up to 60% of the light hitting a thin plated finger can be reflected back in the cell after encapsulation. Burgers also stated light scattering on a rough contact surface such as with screen printed contacts can lead to up to 55% of the light being re-used [BUR99]. According to Burgers, an effective transparency factor for the busbar/tab t_b and for the fingers t_f can be introduced to take into considerations light reflection which leads to the shading fraction of busbar $p_{s,bus}$ and finger $p_{s,f}$:

$$p_{s,bus} = \frac{s \cdot w_{buc}(1-t_b)}{s \cdot a} \tag{4.4}$$

$$p_{s,f} = \frac{w_f(1-t_f)(l_f + w_{buc} t_b)}{s \cdot a} \tag{4.5}$$

and the total shading fraction p_s for plated contacts:

$$p_s = p_{s,f} + p_{s,b} = \frac{s \cdot w_b(1-t_b) + 2 \cdot \left(w_c + 2 \cdot h_f\right)(1-t_f)(l_f + 1/2 \cdot w_b \cdot t_b)}{2 \cdot s \cdot a} \tag{4.6}$$

The total contact area fraction p_{cont} can be calculated by

$$p_{cont} = \frac{s \cdot w_b(1-t_b) + 2 \cdot w_c \cdot (1-t_f)(l_f + 1/2 \cdot w_b \cdot t_b)}{2 \cdot s \cdot a} \tag{4.7}$$

The impact of grid shading on the photo-generated current j_{ph} can be calculated from the photo-generated current without shading j_{ph_nos} and knowing the shading fraction p_s:

$$j_{ph} = j_{ph\_nos} \cdot (1 - p_s) \tag{4.8}$$

Applying equations (4.1) and (4.8) in equation (2.4), the impact of the front metal grid on the two-diode equation can be then calculated from:

$$j(V) = \left(j_{0e,pass} \cdot (1 - p_{cont}) + j_{0e,met} \cdot p_{cont} + j_{0b}\right)\left(\exp\left(\frac{q\cdot(V-|j\cdot r_s|)}{n_1 \cdot k\cdot T}\right) - 1\right) + j_{02}\left(\exp\left(\frac{q\cdot(V-|j\cdot r_s|)}{n_2 \cdot k\cdot T}\right) - 1\right) + \frac{V-|j\cdot r_s|}{r_p} - j_{ph\_nos} \cdot (1 - p_s) \quad (4.9)$$

where the series resistance r_s is obtained from the sum of all individual area-weighted resistance components which are given in Table 4.2.

Following equation (4.9), an optimum needs to be found between series resistance losses, shading losses, and open-circuit voltage losses (J_{01}). In the following, calculations were performed at cell level and at module where for a given contact width w_c the finger separation distance s as well as the finger height h_f were optimized to achieve the maximum efficiency.

Table 4.2: Resistance contributions of a solar cell with an H-grid pattern with a two-layer contact structure at the front and a square pattern of circular points contacts at the rear side with an effective contact radius r_{dot} and separation distance s_{dot}. For the definition of the symbols see Figure 4.2 and Table 4.3.

Resistance	Unit cell [cm^2]	r: area-weighted resistance [Ω.cm^2]
Front emitter [MET07]	I: $a \cdot \frac{s}{2}$	$\frac{1}{12} R_{sh} \frac{(s - w_c)}{l_f} a \cdot s$
Emitter contact [MET07]	I: a $\cdot \frac{s}{2}$	$\frac{\sqrt{R_{sh} \cdot \rho_c}}{l_f} coth\left[\frac{w_c}{2}\sqrt{\frac{R_{sh}}{\rho_c}}\right] a \cdot \frac{s}{2}$
Finger [MET07]	I: a $\cdot \frac{s}{2}$	$\frac{1}{3}\rho_f \frac{l_f}{A_f} as$
Busbar [MET07]	II: $2 \cdot a \cdot b$	$\frac{1}{3}\rho_{bus} \frac{b^2}{h_{bus} \cdot w_{bus}} a$
Tab [MET07]	III: $4 \cdot a \cdot b \cdot N_s$	$\frac{2}{3}\rho_T \frac{a \cdot {l_{bus}}^2}{h_T \cdot w_T}\left[1 + \frac{1}{2{N_s}^2}\right]$
Tab extension [MET07]	III: $4 \cdot a \cdot b \cdot N_s$	$4 \cdot \rho_T \frac{a \cdot b \cdot l_{Te} \cdot N_{sb}}{h_T \cdot w_T}$
Bulk spreading [FIS03]		$\rho_b\left[\frac{{s_{dot}}^2}{2 \cdot \pi \cdot r_{dot}} arctan\left(\frac{2W}{R_{dot}}\right) + W \cdot \left(1 - \exp\left(-\frac{W}{s_{dot}}\right)\right)\right]$
Base contact	${s_{dot}}^2$	$\rho_{rc} \frac{{s_{dot}}^2}{\pi \cdot {r_{dot}}^2}$
Metal layer rear side [MET07]	$2 \cdot a \cdot b \cdot N_s$	$\frac{1}{3}\frac{\rho_{m,rs} \cdot l_f}{h_{m,rs}} a$

Table 4.3: Assumed and calculated parameters for the front grid design optimization.

Assumed parameters		
Symbol	Definition	Used value
A_{cell}	Cell area	156x156 mm^2
j_{ph_nos}	photo-generated current without shading	41.29 mA/cm^2
$j_{0e,pass}$	Emitter dark saturation current density in passivated areas (textured surface)	40 fA/cm^2
$j_{0e,met}$	Emitter dark saturation current density in contact areas (textured surface)	2400 fA/cm^2
j_{0b}	Base and rear side dark saturation current density	117.7 fA/cm^2
j_{02}	Dark saturation current density (n=2)	5x10^{-9} A/cm^2
r_p	Area-weighted shunt resistance	1x10^4 Ω.cm^2
a	length unit cell for 3, 5 or 15 busbars	26 mm; 15.6 mm; 5.2 mm
R_{sh}	Sheet resistance of the emitter	120 Ω/sq
l_f	Finger length for 3, 5, or 15 busbars	25.3 mm; 15.2 mm; 5.1 mm
ρ_{bus}, ρ_f	Resistivity of Cu plated busbars and fingers	1.71x10^{-6} Ω.cm at 25˚C
w_{bus}= w_T	Busbar width = tab width for 3, 5, or 15 busbars	1.5 mm, 0.9 mm, 0.2 mm
b	Width unit cell II	0.64 mm
ρ_T	Resistivity of Cu tab	1.71x10^{-6} Ω.cm at 25˚C
l_{bus}	Busbar length	154 mm
h_T	Tab height	0.2 mm
N_{sb}	Number of solder joints per busbar	12
l_{Te}	Length of tab extension	5 mm
ρ_b	Bulk resistivity	1.47 Ω.cm
s_{dot}	Spacing between rear point contacts	0.6 mm
r_{dot}	Effective rear contact radius	72.45 µm
W	Wafer thickness	160 µm
ρ_{rc}	Specific contact resistance of Al rear contact	0.1 mΩ.cm^2
$\rho_{m,rs}$	Resistivity of metal rear side (Al)	2.71x10^{-6} Ω.cm at 25˚C
$h_{m,rs}$	Rear Al thickness	2 µm
t_f, t_b	Transparency factor of fingers/busbars	0 %

Calculated parameters		
Symbol	Definition	Used value
s	Finger separation distance	variable
h_f=h_{bus}	Finger height ≈ Busbar height ≈ plating height	variable
ρ_c	Specific contact resistance of Ni	variable in Fig. 4.4, 0.5 mΩ.cm^2 in other figures

4.2.2. Results at cell level

Current-voltage measurements of a single solar cell are typically performed using a conductive chuck and a set of closely spaced pins that collect the current at the front busbars. Such measurements neglect the effect of resistance in the busbar, tab, tab extension, and rear side metal layer. These resistances are independent of finger width and the finger separation distance (compare Table 4.2) and hence do not influence the front grid optimization.

We simulated the efficiency of an i-PERC device featuring a high-efficiency 120 Ω/sq homogenous deep emitter. The assumed parameters for this device are given in Table 4.3. The dark saturation current density j_{0b}=117.7 fA/cm^2 corresponds to the previously mentioned effective rear surface recombination velocity of 70 cm/s and bulk lifetime of 1500 µs that are typical for i-PERC devices in this work. The high-efficiency 120 Ω/sq homogenous deep emitter is sensitive to recombination under the front contacts which is characterized by a high $j_{0e,met}$=2400 fA/cm^2. For consistency, shunt resistance, wafer thickness, base doping, and j_{02} recombination were taken identical to the PC1D simulations mentioned earlier (see Table 4.1).

The influence of the specific contact resistance of the contact layer was evaluated for various contact widths as shown in Figure 4.5. The advantage of narrow contact widths is particularly obvious because of the high sheet resistance of the emitter which requires narrow finger spacing to minimize the emitter resistance loss. As the contact width is decreased, the grid shading losses are decreased. From this data, the specific contact resistance should be as small as possible to enable the use of narrow contact widths and maximize cell efficiencies. In practice, contacts widths as low as 8 µm can be achieved with laser ablation and hence the contact resistivity should be below 0.5 mΩ.cm^2 so that its impact on efficiency is less than 0.1% abs.

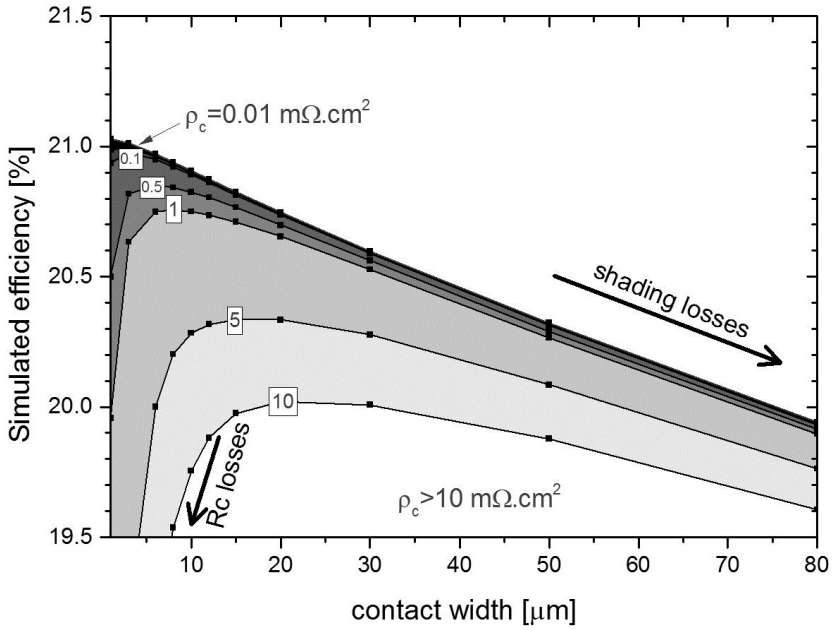


Figure 4.5: Simulated efficiency as a function of specific contact resistance for an i-PERC solar cell with 3 busbars featuring a 120 Ω/sq emitter and using the parameters given in Table 4.3.

4.2.3. Results at module level

In the previous calculations resistance losses in the busbar, tab, and rear side metal layer were not taken into considerations. However, they have a strong impact on module efficiency since the current needs to be carried out by the busbar to the tab and to the next cell in the string.

A high number of soldering joints between the busbar and the tab is required to minimize the resistive loss in the busbar. Similarly wider and thicker tabs are preferred to minimize the resistive loss in the tab. However, thicker tabs tend to impart more stress on the busbar and can lead to module failure upon thermal cycling. Tabs wider than the busbars will also increase shading losses and hence will impact the front grid optimization.

In a first calculation we assumed tinned (Sn/Ag/Pb) copper tabs as typically used in industrial environment which are 200 µm thick and 1.5 mm wide. Calculations were performed for a 3 busbars cell assuming a contact resistivity of 0.5 mΩ.cm^2 and using the same parameters as before (Table 4.3). From the results given in Figure 4.6, the busbar, tab, and rear side metal layer introduce an additional series resistance of ~0.29 Ω.cm^2 which leads to ~1.5%$_{abs}$. drop in fill factor and consequently a 0.4%$_{abs}$ drop in efficiency. In this 0.29 Ω.cm^2, the busbar accounts for ~0.01 Ω.cm^2 and the 2 µm thick rear Al layer for ~0.03 Ω.cm^2 which shows that most of the resistive loss is in the tab itself. Short-circuit current densities at cell and at module level are practically the same (no absorption/reflection loss in glass/encapsulant is assumed) demonstrating that r_s losses in busbar, tab, and rear Al layer have no impact on the front grid optimization. Assuming a transparency factor of 60% for the fingers at module level, j_{sc} increases by up to 0.4 mA/cm^2 for narrow contact widths leading to a efficiency gain of up to ~0.3%$_{abs}$. The gain is only ~0.1 mA/cm^2 for 80 µm contact widths which clearly outlines the advantage of narrow contact widths.

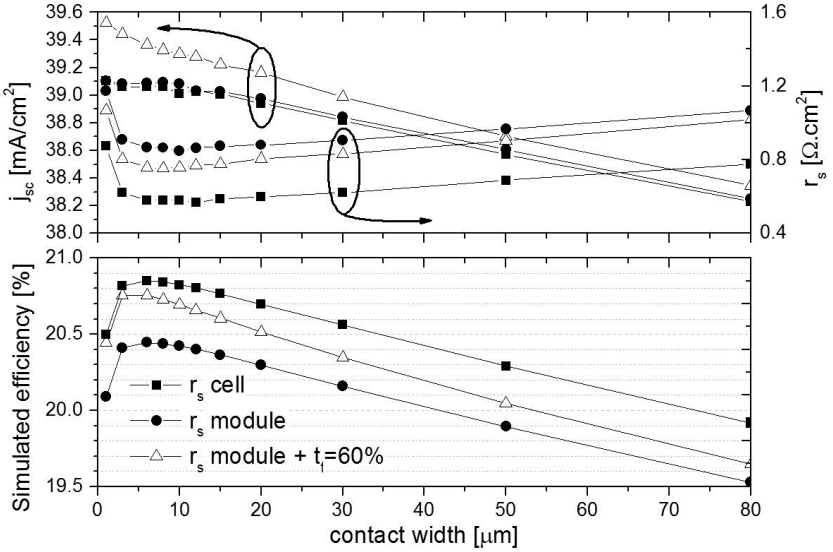


Figure 4.6: Simulated efficiency at cell level, at module level (series resistances in busbar, tab, and rear metal layer included), and at module level assuming a finger transparency factor of 60% [BLA92].

A high number of busbars is beneficial as this decreases the length a of unit cell I (see Figure 4.2b) which lowers the resistive loss in both the fingers and the busbars (see Table 4.2). This triggered the move in industry from 2x 2 mm wide busbars to 3x1.5 mm wide busbars which are now standard on 156x156 mm^2 substrates. Similarly, moving from 3x 1.5 mm wide busbars to 5x 1 mm wide busbars, a small gain can be expected as the plated thickness can be re-optimized. This is shown in Figure 4.7 where a ~0.1%$_{abs}$ gain is calculated despite a 0.3%$_{abs}$ increase in busbar area. It can be explained by the shorter finger length which allows to reduce the plated thickness from ~12 µm down to ~8 µm cancelling out the increase in shading from the busbar (j_{sc} with 3x 1.5 mm and 5x 1 mm busbars are identical) and still enabling a reduction in resistive losses. As plating time is linear with plated thickness, a 33% reduction in process time is expected which allows for either faster throughputs or a smaller/cheaper plating equipment. Going further, as the present i-PERC cell is limited by recombination under the front contacts, a 9 mV gain in V_{oc} is calculated by using busbars which are only in contact with the fingers (also called floating busbars). The use of floating busbars reduces the contact area by ~50% and translates in a 0.3%$_{abs.}$ gain in efficiency compared to fully-contacted case. Finally, efficiencies can be improved from 20.8% for a cell with 3x 1.5 mm busbars and 10 µm contact widths to 21.4% if 15x 0.2 mm wide round multi-wires (see chapter 3.3) are implemented. In the latter case, non-only the wires are floating and closely spaced but they are assumed to reflect 70% of the light back in the cell [BRA13]. As a result the use of multi-wires leads to a 1.2 mA/cm^2 gain in j_{sc} and a ~75% reduction in plating time compared to the original 3x 1.5 mm busbars.

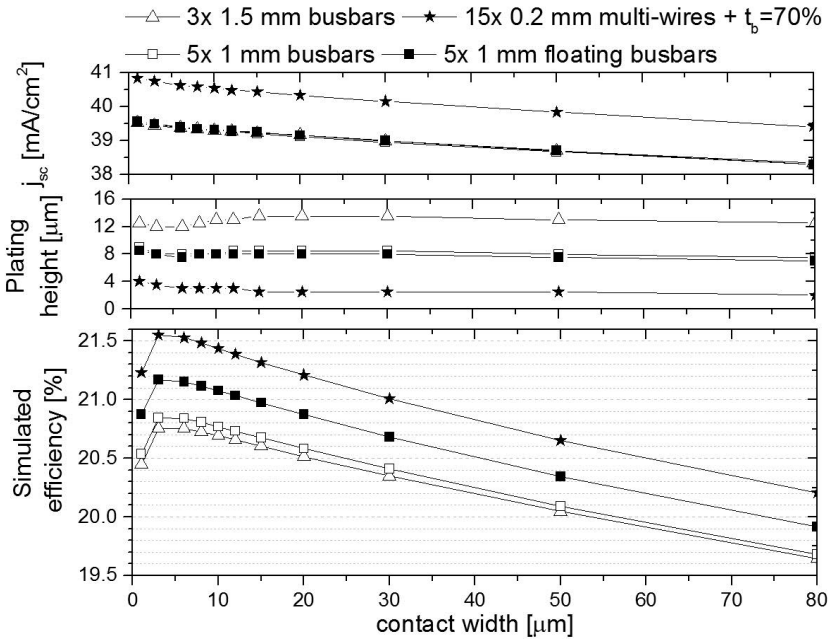


Figure 4.7: Simulated efficiency at module level assuming a finger transparency factor of 60% for 3x 1.5 mm busbars, 5x 1mm busbars, 5x 1 mm floating busbars, and 15x 0.2 mm multi-wires. For busbars, transparency factor was kept to 0% while for wires it was assumed to be 70%.

4.3. Chapter summary

In this chapter, basic simulations were performed to evaluate the impact of front emitter design and front metal grid design. Lowly doped emitters (~120 Ω/sq) were shown to have a high efficiency potential. The advantage of narrow contact widths was demonstrated. The analytical model presented enables an optimization of the front grid design (plated height, finger separation distance) which includes the impact of recombination at the metal-contact on the open-circuit voltage.

Based on these simulations, self-aligned nickel/copper plated contacts should meet the electrical and design requirements defined in Table 4.4 in order to enable industrial high efficiency silicon solar cells.

Of particular importance are the low $j_{02} < 5x10^{-9}$ A/cm^2 and specific contact resistance $\rho_c < 0.5$ mΩ.cm^2 which are required to achieve high fill factors >80%. We will see that j_{02} values are strongly dependent on damage created during the metallization sequence and the emitter depth. Similarly, the specific contact resistance will be dependent on the emitter surface concentration, surface preparation prior to nickel deposition, and nickel silicide formation. Therefore, a co-optimization of the nickel/copper metallization sequence and the emitter profile shape is required.

Finally, grid design simulations were performed at module level to include the effect of resistances in the busbar, tab, and rear side metal layer. Instead of using a 3x 1.5mm busbar front grid design, 5x 1mm floating busbars, or 15x 0.2mm multi-wires were shown to present a strong efficiency potential. In addition, such approaches were shown to enable drastic reduction in plating time.

Table 4.4: Electrical and design requirements for nickel/copper plated front side contacts

Parameters	Target value	unit
j_{02} recombination (n=2)	$< 5x10^{-9}$	A/cm^2
Specific contact resistance of front contact layer	< 0.5	mΩ.cm^2
Resistivity of Cu plated busbars and fingers	~$1.71x10^{-6}$	Ω.cm
Contact width	< 15	µm
Plated thickness for 3, 5, 15 busbars (120 Ω/sq emitter)	12, 8, 3	µm

CHAPTER 5

Towards p-type i-PERC Si solar cells with fully plated contacts

In this chapter we first evaluate ns-UV laser ablation of the front SiN_x anti-reflective coating as an alternative to photolithography (wet etch) patterning using various sputtered metal seed layers defined by lift-off. In the second part of this chapter, sputtered Ni seed layers are investigated and front contacts are defined using a self-aligned silicide (SALICIDE) process. Electroless deposition and bias-assisted light-induced plating (LIP) of nickel are then evaluated as an alternative to PVD Ni. Finally, a simplified "litho-free" sequence is described for the definition of fully plated front contacts and results are demonstrated on industrial size (15.6x15.6 cm^2) p-type i-PERC solar cells using pilot production plating and sintering tools.

5.1. Evaluation of CMOS metal barriers

5.1.1. Background on front dielectric(s) patterning

In order to obtain highly efficient solar cells, it is crucial to define contact openings in the front anti-reflective coating (ARC) without damaging underlying silicon. Defects extending into the p-n junction should be avoided as they lead to higher j_{02} recombination. To be compatible with mass-production, the patterning technique must be reliable, high-throughput, and low-cost.

Photolithography patterning, as used in laboratory cells with Ti/Pd/Ag evaporated contacts (see Chapter 3.2.1), enables the removal of the ARC layer by an etchant (typically buffered HF is used to etch SiN_x) and hence leads to negligible damage to the underlying silicon. However, photolithography patterning is not suited for mass-production due to its cost.

Alternative front ARC patterning techniques such as laser ablation or laser-doped selective emitters (LDSE) enable: (i) direct removal of the front ARC, (ii) ultra-fine line (down to ~10 µm wide openings), and (iii) can offer short processing time (few seconds per wafer). To the best knowledge of the author, laser ablation of the SiN_x ARC layer on the front textured side was first applied by Dubé and Gonsiorawski [DUB90] in 1990 in a seed-and-plate approach. The mechanism for laser ablation of dielectric layers has been described as a "lift-off" mechanism or as "partial lift-off" mechanism [HEI11].

In the "lift-off" mechanism, which has been reported for a wide variety of pulse wavelengths and pulse durations, the incident photon energy is absorbed in Si which melts locally and lifts-off the dielectric layer(s) if the vapor pressure of molten Si is sufficient to break the layer(s) [HER10a]. As a result, ablation thresholds are expected to vary depending on the mechanical strength of the dielectric layer which can be influenced by its type (thermal oxide, PECVD SiN_x) and thickness. Also, intrinsic stress has been reported to play a role in ablation

with compressive SiN_x layers (typically obtained with direct PECVD systems) being ablated more readily than tensile ones (remote PECVD) [ENG13]. Amorphous Si (a-Si) is typically found underneath the ablated areas due to fast resolidification leading to incomplete recrystallization [HER10b]. For pulse durations in the nanosecond (ns) range, laser-silicon interaction is sufficiently long to allow heat diffusion thus leading to dopant redistribution in the emitter and to reduced sheet resistance values if inactive dopants become electrically active [KNO09a]. On the contrary, ultrashort pulse durations (in the picosecond (ps) or femtosecond (fs) range) lead to a shallow heat affected zone particularly for short wavelengths lasers. In this case, higher sheet resistance values are found in the ablated areas due to material removal and the presence of a-Si in the topmost region [KNO09a, HEI11, GAL13].

In the current explanation for ”partial lift-off” mechanism, direct absorption in the dielectric layer(s) is achieved by avalanche ionization which leads to heating and vaporization of the dielectric layer(s) [HEI13]. Partial lift-off have been reported for SiN_x layers on planar Si with ps-visible (VIS) (λ=532 nm) [HEI11] and ps-infrared (IR) (λ=1025 nm) pulses [HEI13].

There has been report of ns-UV (λ=355 nm) laser pulses ablating SiN_x or SiO_2 layers without appreciable damage to the underlying silicon on planar surfaces [ENG07, KNO09b, HER10b]. However, alkaline textured surfaces have been reported to suffer from laser-induced damage (reduction in lifetime) due to light trapping effects at the tips and the edges of the pyramids leading to non-homogeneous laser irradiation [KNO09b]. In front junction devices, extended crystal defects (dislocations) causing an increase in j_{02} recombination were reported for the front laser ablation of SiN_x layers with ps-VIS laser pulses on alkaline textured surfaces and were attributed to slower recrystallization speeds on the pyramid side walls (111) than on planar (100) Si and/or to the above mentioned light-trapping effects leading to thermal stress [HER10b]. Recently, solar cell results were published comparing ns- and ps-UV laser ablation of the front SiN_x on alkaline textured surfaces in a seed-and-plate approach with Ni/Ag contacts. The results showed a 17 mV higher open circuit voltage in case of the ns-UV laser, which was explained by emitter profile modifications and varying metallization fractions [KNO09a].

5.1.2. Solar cell processing

A wide variety of metals acting as diffusion barriers against copper diffusion can be deposited by evaporation, sputtering, or chemical vapor deposition (CVD). In complementary metal oxide semiconductor (CMOS) devices, the metal layers chosen as diffusion barriers against Cu diffusion should primary exhibit low electrical resistivity and sufficient adhesion to Cu and the surrounding inter layer dielectrics (see Chapter 3.2.4). In order to serve both the function of diffusion barrier and contact layer in silicon solar cells, these metals should additionally offer low contact resistance to lowly doped silicon and sufficient adhesion to silicon.

Large area CZ-Si substrates were processed into i-PERC solar cells with different contact/barrier materials according to the sequence given in Figure 5.1.

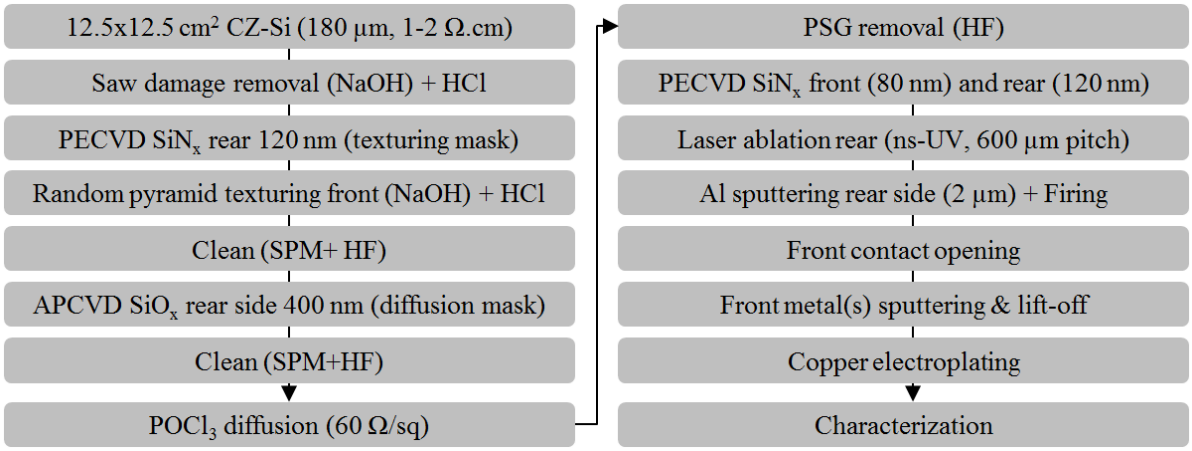


Figure 5.1: Process sequence diagram for p-type i-PERC solar cells with copper plated front contacts.

After a saw damage removal step (~10 µm Si removal per side) in NaOH and a subsequent neutralization step in diluted HCl, the wafers were random pyramid textured on one side (~10 µm Si removal) using a SiN_x texturing mask deposited by plasma-enhanced CVD. Wafers were then cleaned in a sulfuric peroxide mixture (SPM: H_2O_2:H_2SO_4 1:4) followed by a long dip in diluted HF which resulted in the removal of the SiN_x texturing mask. A thick SiO_x diffusion mask was applied at the rear side by atmospheric pressure CVD (APCVD) prior to $POCl_3$ diffusion. The thick APCVD SiO_x was kept through the subsequent phosphorous silicate glass (PSG) removal in HF and served as rear passivation layer. A SiN_x capping (n=2.1) at the rear and a SiN_x anti-reflective coating (ARC) (n=2.1) at the front were applied by PECVD. Points contacts openings were defined at the rear using a ns-UV laser, a thin (2 µm) Al layer was sputtered, and local Al back surface field (Al-BSF) regions were formed by high temperature firing (~800˚C for a few seconds) in a belt furnace.

At this stage, the front contact structure was defined by locally opening the ARC either by laser ablation or using a photolithography wet-etching sequence. Front metal contacts were then defined by lift-off (see Chapter 3.2.1) of a stack of metals (barrier + seed). While the same photo-resist was used for patterning the ARC and performing metal lift-off, precise alignment was required between the laser openings in the ARC and the metal lift-off pattern. Though rather complex, this approach gave the possibility to evaluate laser patterning of the front ARC together with thin (~30nm) sputtered metal layers which are either known in CMOS for their contact/adhesion properties (e.g. Ti, Ni) or for being excellent barrier to Cu diffusion (e.g. Ta, TiN, TaN). In addition, this approach also solved any non-uniformity issues during the subsequent Cu electroplating step (thickness~10 µm) as a thin (150nm) Cu seed layer, ensuring sufficient conductivity, was sputtered on top of the barrier layer prior to lift-off.

5.1.3. Initial developments of front dielectric(s) patterning at imec

Based on literature study and laser platforms initially available at imec, process developments for the patterning of the SiN_x ARC on alkaline textured surfaces were started using

a 355 nm Nd-YVO_4 ns-laser (Trumpf TruMark 6330, pulse duration~13 ns at 75 kHz repetition rate). Solar cells were processed according to the sequence given in Figure 5.1. The laser repetition rate was kept constant at 75 KHz, the laser pulse energy was varied by changing the percentage of power attenuation, and the scanning speed was optimized in order to maintain a constant 25% pulse overlap. The ablation threshold of the SiN_x ARC layer was determined using optical microscopy and scanning electron microscopy (SEM). From the optical inspection (Figure 5.2a), pulse energies below 5 µJ lead to incomplete SiN_x removal and extended line discontinuities. For pulse energies above 7.5 µJ, the average ablated line width increases with pulse energy which is expected for a Gaussian beam profile [HER10b]. However, the alkaline texture appears to be destroyed in some areas due to severe Si melting particularly for pulse energies above 12 µJ. From SEM pictures, SiN_x is found to be preferentially ablated at pyramid tips and edges as expected from literature. Even for low pulse energies, molten pyramid tips are observed while SiN_x removal is incomplete in pyramid facets as shown in Figure 5.3a. Laser-induced damage was then investigated by means of Suns-Voc measurements performed directly after the ns-UV ablation process. For laser pulse energies above 12 µJ, measured Suns-V_{oc} values, as shown in Figure 5.3b, drop below 620 mV indicating an increased in surface and bulk emitter recombination (increased j_{01}).

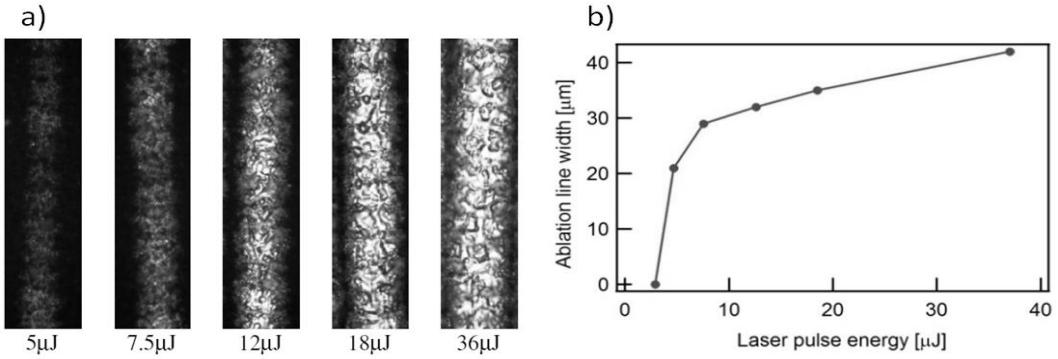


Figure 5.2: a) Optical pictures of ablated lines at different pulse energies. b) Average ablated line width as function of laser pulse energy.

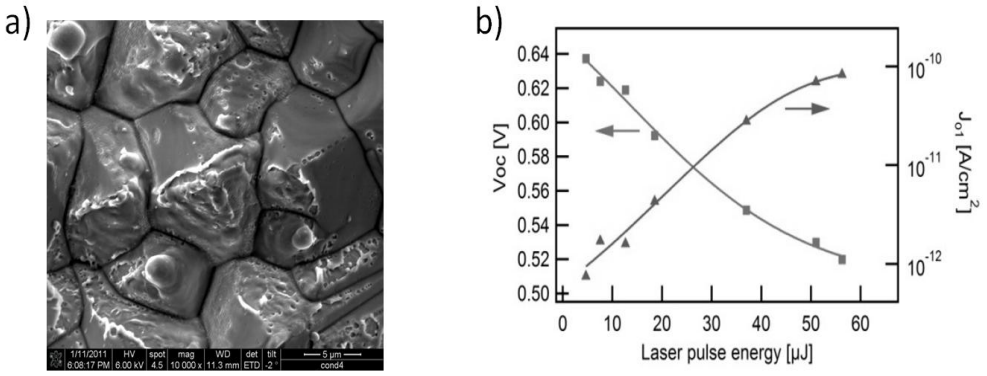


Figure 5.3: a) Scanning electron microscopy of a ns-UV laser-ablated finger area (5 µJ/pulse, 75 KHz, 112.5 mm/s scanning speed. b) Suns-Voc and j_{01} obtained from Suns-Voc measurements directly after the laser ablation process.

In a first iteration, a sputtered Ti/Cu stack was chosen to evaluate laser ablation of the front ARC at solar cell level. Based on previous findings, laser ablation was performed at 75 KHz repetition rate and using a pulse energy of 5 µJ to minimize laser-induced damage. As shown in Figure 5.4, three ARC opening patterns were tested: point contacts (PC) ns-UV laser openings, line contacts (LC) ns-UV laser openings, and the reference wet-etched (WE) openings. The calculated percentage of contacted areas varies from 0.4% for PC (100 µm dot pitch), to 3.8% for LC, and to 8.0% for WE. Average energy conversion efficiencies around 18.2% were obtained with PC and LC samples (~18% with WE samples) as shown in Figure 5.5. All three groups gave comparable short circuit current densities (j_{sc}~37.2 mA/cm^2) as expected from the identical lift-off grid design (2 busbars H-pattern, 100 µm wide fingers, 1.5 mm finger pitch) leading to identical shading losses. The open-circuit voltages values were 3-4 mV higher for PC that for WE samples which can be explained by the reduction in contacted areas leading to a reduction in front side recombination. Comparable fill factors (FF~77%) and pseudo fill factors (pFF~82%, not shown) were measured for all three groups which indicates that i) the specific contact resistance of Ti is sufficiently low to allow narrower contact openings and ii) laser ablation of SiN_x does not lead to an increase in j_{02} recombination as compared to WE samples.

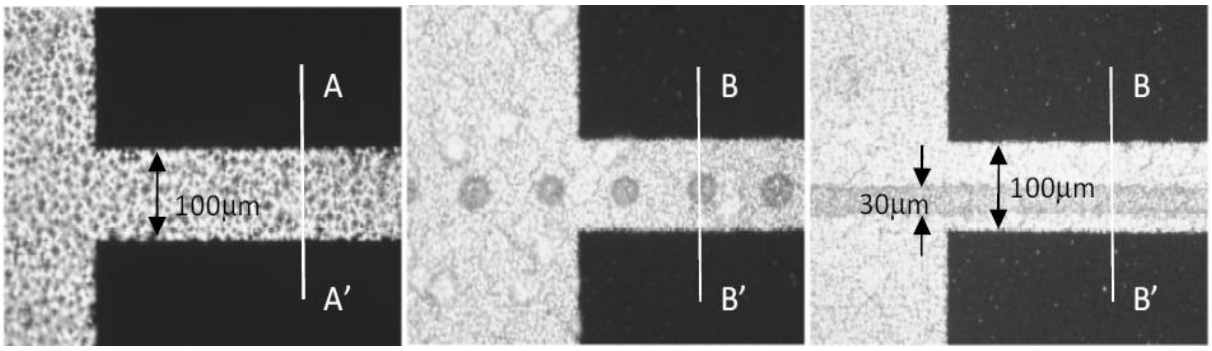


Figure 5.4: From left to right: reference Ti/Cu contacts with wet etched (WE) pattern, Ti/Cu contacts aligned to point contacts (PC) ns-UV laser openings, Ti/Cu contacts aligned to line contacts (LC) ns-UV laser openings.

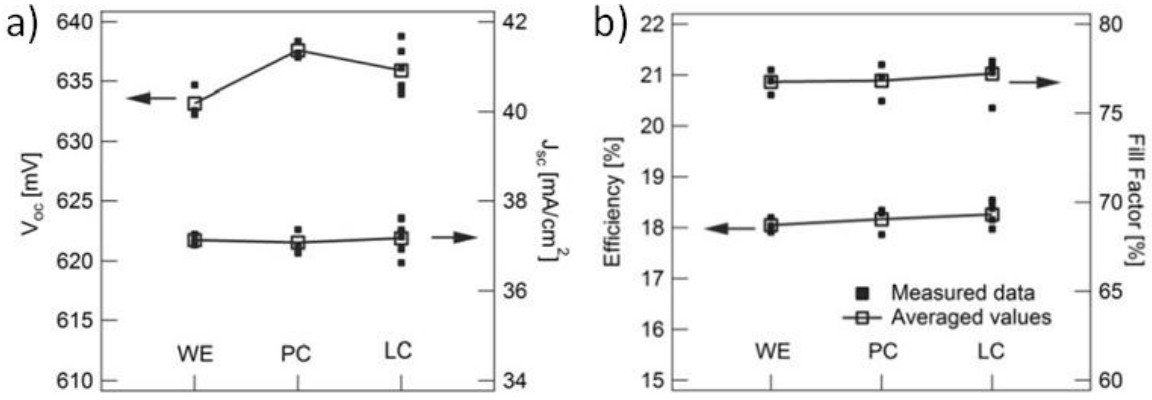


Figure 5.5: a) Efficiency and fill factor results for i-PERC solar cells with wet etched (WE), point contacts (PC) or line contacts (LC) openings and Ti/Cu metallization. b) Open-circuit voltage and short-circuit densities results for the same cells as in a).

In a second iteration, point contacts ns-UV laser openings were used in combination with various barrier metals (Ti/TiN, Ta, TaN, Ni) deposited by sputtering . In an attempt to minimize shading losses, the finger width of the lift-off pattern was reduced from 100 μm down to 40 μm keeping the same 1.5 mm finger pitch and 10 μm Cu plating thickness. Energy conversion efficiencies around 19% were obtained for the different barrier metals as shown in Table 5.1. The higher efficiencies are the result of ~1mA/cm^2 higher short-circuit current densities as compared to previous results which can fully be attributed to the reduction in shading percentage (from 8% down to 5.5%). The open-circuit voltage and fill factor values are comparable for all barrier metals and are in line with the values obtained in the previous experiment. This indicates that the point contact ns-UV laser ablation process is reproducible and that fill factors are not limited by finger resistance since the Cu plated fingers are narrower than before.

Table 5.1: Illuminated I-V parameters of best large area (A=148.6 cm^2) p-type, CZ-Si, i-PERC solar cells with point contacts ns-UV laser openings and various barrier layers deposited by sputtering.

barrier layer	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	ŋ [%]	r_s [Ohm.cm^2]
Ti/TiN	38.1	638	77.7	18.9	0.76
Ta	38.2	640	77.9	19.0	0.82
TaN	38.3	636	77.8	19.0	0.78
Ni	38.3	639	77.7	19.0	0.69

From these two experiments, it can be concluded that front side ns-UV laser ablation of SiN_x can be performed without significant damage in the case of a 60 Ω/sq emitter since relatively high fill factors were measured. In addition, sputtered Ni was shown to lead to comparable performance as with a standard Ti barrier layer indicating that Ni offers sufficiently low contact resistance on a conventional 60 Ω/sq emitter.

These two developments open the way towards lithography-free solar cells with Ni/Cu contacts since self-aligned nickel silicide contacts (SALICIDE) can be performed by Ni sputtering, sintering at relatively low temperature, and unreacted Ni removal. However, laser ablation of the front ARC might favor diffusion of metal into the junction upon contact sintering particularly as one moves to high efficiency emitters which are shallower than the current 60 Ω/sq emitter. Therefore, detailed investigations are performed in the next sections to clarify this.

5.2. Evaluation of sputtered Ni seed layers

5.2.1. Background on self-aligned silicides

Nickel silicides can be formed by solid-state reactions between Ni and Si, by co-deposition [GAM98], and also by liquid-state reactions (see Chapter 9). As shown in Figure 5.6, the Ni-Si phase diagram is relatively complex with eleven phases, six of which are stable at room temperature (Ni_3Si , $Ni_{31}Si_{12}$, Ni_2Si , Ni_3Si_2, NiSi, and $NiSi_2$).

For thin Ni films (~10-50 nm in IC industry) on thick Si substrates (Si supply is not limiting the reaction), early work, based on *ex-situ* measurements at room temperature after rapid thermal annealing, suggested a simple $Ni_2Si \rightarrow NiSi \rightarrow NiSi_2$ phase sequence with the new phase beginning to grow after the most metal-rich is consumed [DEN97, GAM98, LAU04, KIT08]. The formation of Ni_2Si, NiSi, $NiSi_2$ has been observed at different temperatures (250-300°C, 300-700°C and >700°C respectively) with nickel being the main diffusing species and silicide formation being diffusion or interface limited [GAM98, LAU04, KIT08]. More recently, *in-situ* x-ray diffraction (XRD) during ramp annealings enabled the detection of phases that only exist in limited temperature ranges and revealed a more complex Ni-rich silicide phase sequence with transient formation of other Ni-rich silicides at initial stages of the reaction [LAV03, RIV05].

In contrast, for cases in which the Si supply is limited (e.g. Ni/100 nm polycrystalline-Si/SiO_2 gate stack as shown in Figure 3.10 in Chapter 3), solid-state reactions were shown to result in the formation of Ni-rich silicides as end phases [KIT07, VAN09].

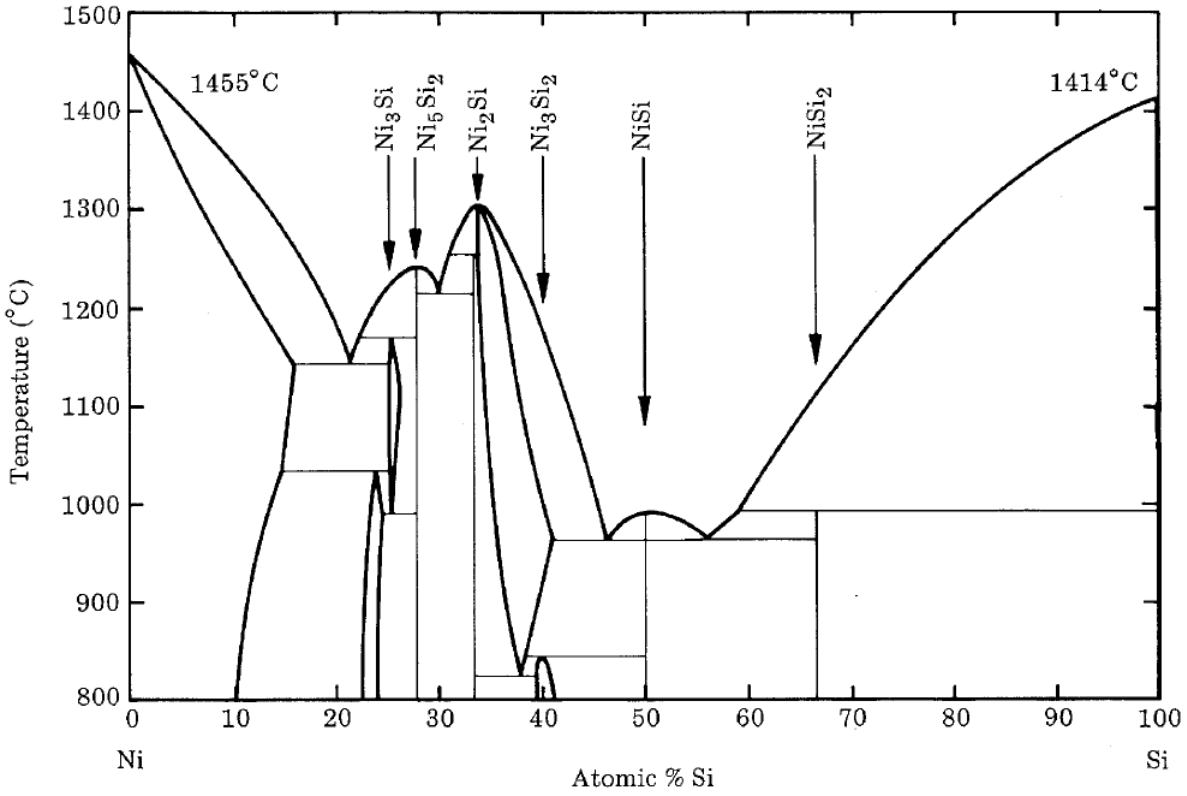


Figure 5.6: Ni-Si phase diagram [GAM98].

If the diffusion of nickel is altered by impurities, nickel silicide formation might behave considerably differently. Impurities can be: (i) films at the Ni-Si interface due to native oxides or contamination, (ii) contaminants in the nickel film from either the metal deposition (e.g. phosphorous in electroless Ni, see next section 5.3) or from the annealing ambient (e.g. oxygen or nitrogen), or (iii) dopants in the Si substrate. Oxygen in Ni films results in high resistivity of the Ni-silicide film, poor thermal stability, and poor electrical interface which usually results in leakage current increase. As a result, annealing is usually performed in pure nitrogen ambient ($[O_2]$ < 5ppm) since nitrogen does not react with Ni at temperatures used for silicidation [GAM98]. Native oxide or interfacial oxide (chemically or thermally grown) of about 2 nm have been reported to inhibit nickel silicide formation up to temperatures of 800˚C [LEE00, TAN02]. On the contrary, direct formation of $NiSi_2$ pyramids by diffusion of Ni through a thin (<1 nm) chemical oxide at temperatures as low as 150˚C has also been reported [TEO01]. Solutions introduced to improve reproducibility include minimizing time lag between native oxide removal (HF-dip) and nickel deposition, using in-situ pre-clean (plasma-clean), or sputtering a Ti or TiN cap on top of Ni prior to silicidation. Titanium can diffuse through Ni and is capable of reducing interfacial oxide [TAN02]. The transformation from the Ni_2Si to the NiSi phase on arsenic (n-type) and boron (p-type) samples was found to be slightly delayed as compared to non-doped samples [LAU01]. Also dopant pile-up at the NiSi/Si interface, thereby reducing contact resistance, was evidenced by SIMS measurements [IWA02,FOG04]. The transformation from the NiSi phase to the higher resistive phase $NiSi_2$ (not-desired) have been reported to be delayed by alloying Ni with metals such as Pt or Al [KIT08, LEE08]. In addition, NiAl-alloy silicides were shown to exhibit considerably lower barrier height on n-doped (100) Si than NiSi [LEE08].

In IC industry, NiSi is the preferred phase since it offers the lowest resistivity (see Chapter 3.2.5). Nickel silicide formation does not occur at the dielectric regions (isolation, spacers) separating the contacts regions and a subsequent selective etch removes unreacted nickel leaving behind the self-aligned silicide contacts (SALICIDE). Selective etching of unreacted nickel has been reported using dilute sulfuric peroxide mixtures (SPM: H_2SO_4:H_2O_2) or nitric acid (HNO_3) since both chemistries do not attack silicon nitride (spacers) or silicon oxide (isolation) [GAM98]. The NiSi versus Ni selectivity of SPM and HNO_3 chemistries is based on the fact that oxidation and dissolution of unreacted Ni stops when a silicon oxide layer is formed on top of the silicide [CAR07]. For NiPt-alloy silicides or for Ge-rich NiSiGe alloys, alternative chemistries are required to achieve selectivity [CAR07, IMB08].

One challenge is to control nickel silicide formation as to obtain to desired phase without degrading device performance. Metrics for device performance are junction leakage (measured in reserved bias) in IC industry and j_{02} recombination (measured in forward bias) for solar cell devices, both of which should be kept as low as possible. In IC industry where devices are created on defect-free planar (100) Si using photolithography patterning and junction depths are often found below 100 nm, increased junction leakage has been attributed to silicide spikes [KUD08], interfacial roughness [FOG04], and to clustering of Ni atoms released from NiSi during silicidation [TSU04]. Reducing Ni thickness was found to reduce junction leakage as this

reduces NiSi depth [FOG04]. Two-step rapid thermal annealing (RTA) processes were shown to reduce leakage by reducing excessive silicidation at the edges of the contact areas (source/drain) due to Ni diffusing from the surrounding areas (isolation, spacers) [LAU04, FOG04, HAI09]. In the two-step RTA approach, the thermal budget) of RTA1 is tuned (low temperature and/or short annealing time) to form only a thin Ni_2Si. Subsequently, excess Ni is removed using a selective etch, and Ni_2Si is converted into NiSi during RTA2. Reducing the temperature of NiSi formation to below 450˚C was also suggested to minimize the effect of atomic Ni diffusion [TSU04].

A key element for silicon solar cells is that crystal defects (e.g. laser-induced damage on alkaline textured surfaces, scratches, defects generated during diffusion/passivation) might enhance nickel diffusion and hence junction degradation. Also, solar cells are large area diodes and hence are more subjected to local shunts. Finally, specific contact resistance requirements are different ($<1x10^{-6}$ Ω.cm^2 in IC industry, $< 5x10^{-4}$ Ω.cm^2 for 10 µm wide contacts in PV) and hence the lowly resistive NiSi phase might not be required.

5.2.2. Application of nickel SALICIDE to silicon solar cells

We first evaluated the impact of Ni thickness, sintering temperature, and sintering duration on nickel silicide formation using high resistivity mirror polished 700 µm thick 200 mm diameter CZ-Si samples as used in IC industry. Native oxide was removed in 1% HF prior to nickel sputtering in a NEXX Nimbus310 system (pure 5N Ni target, sputtering power 1200 W, deposition rate: ~30 nm/min). Various Ni thicknesses (30, 50, 70, and 90 nm) were deposited by varying the deposition time from 60s to 150s. Deposited thicknesses were extracted from 4 point probe sheet measurements knowing resistivity ($\rho_{Ni,PVD}$=11.7 µΩ.cm at 25˚C) and thickness of an etalon sample. Samples were cut into 4x4 cm^2 pieces and rapid thermal annealing was performed in a manual rapid thermal annealing (RTA) tool (AccuThermo AW 610) under constant flow of nitrogen (10 liters/min, [O2] <5 ppm). After RTA, unreacted Ni was removed in H_2SO_4:H_2O_2.

Sheet resistance measurements versus RTA peak temperature (steady time at peak temperature = 30s) are shown in Figure 5.7a for different Ni thicknesses. Nickel silicides are formed at temperatures as low as 275˚C. Rutherford backscattering (RBS) measurements indicate the formation of Ni_2Si only at 275 ˚C and of mixture of both Ni_2Si and NiSi phases at 350 ˚C. The sheet resistance drops until Ni_2Si is fully converted to the low resistive NiSi phase which is stable between 400 and 600 ˚C. At 600 ˚C, NiSi starts to agglomerate into $NiSi_2$ which is about 3x more resistive and hence sheet resistance increases again. The range of temperatures for silicide formation correspond fairly well with literature data described earlier. Higher sheet resistance values obtained at 500 ˚C with thinner Ni layers also correspond well with the fact that NiSi thickness is controlled by the deposited Ni thickness. Finally, the influence of sintering time at 450˚C was evaluated as shown in Figure 5.7b. From this data, 30s steady time at peak temperature appear to be sufficient to fully convert Ni into NiSi for thin Ni layers (Ni< 70 nm).

Sheet resistance measurements were performed on alkaline textured wafers (p-type,1-2 Ω.cm, 160 µm thick) to simulate nickel silicide formation on solar cells substrates. RTA

temperature and Ni thickness were fixed to 30s and 40 nm respectively. From the sheet resistance results given in Figure 5.8a, we can confirm that nickel silicides are formed at low temperatures and that below 300˚C the deposited Ni layer is not fully reacted since the sheet resistance increases after unreacted Ni removal. The fact that Ni_2Si is formed at temperatures as low as 250˚C is possibly due to the thinner substrates heating faster or to a better native oxide removal prior to Ni deposition. Assuming a resistivity of 24 μΩ.cm at 25˚C for Ni_2Si (obtained from RBS thickness measurements), we find that the square of the estimated Ni_2Si thicknesses is linear with RTA temperature at 275°C and at 300°C as shown in Figure 5.8b. This confirms that Ni_2Si formation is diffusion-limited. It is interesting to remark how much faster the estimated Ni_2Si thickness increases with RTA time at 300°C as compared to 275°C. From this data, low RTA temperature (275°C or below) would be preferred to accurately control the Ni_2Si thickness.

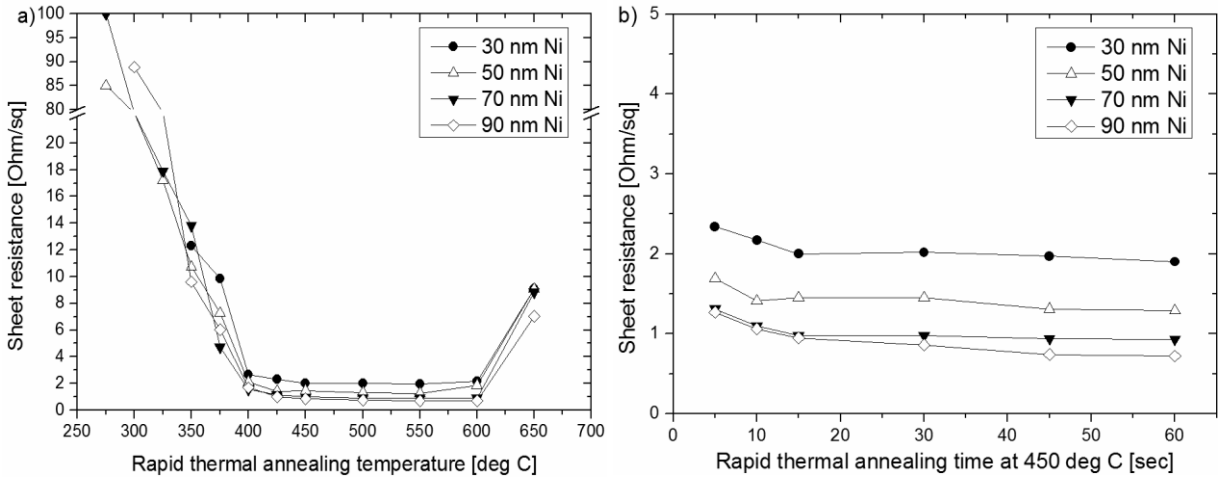


Figure 5.7: a) Sheet resistance of nickel silicides on mirror-polished 700 μm p-type CZ-Si as a function of rapid thermal annealing (RTA) temperature for various sputtered Ni thickness. b) Influence of RTA time at a peak temperature of 450˚C for various sputtered Ni thickness on the same mirror-polished 700 μm p-type CZ-Si wafers.

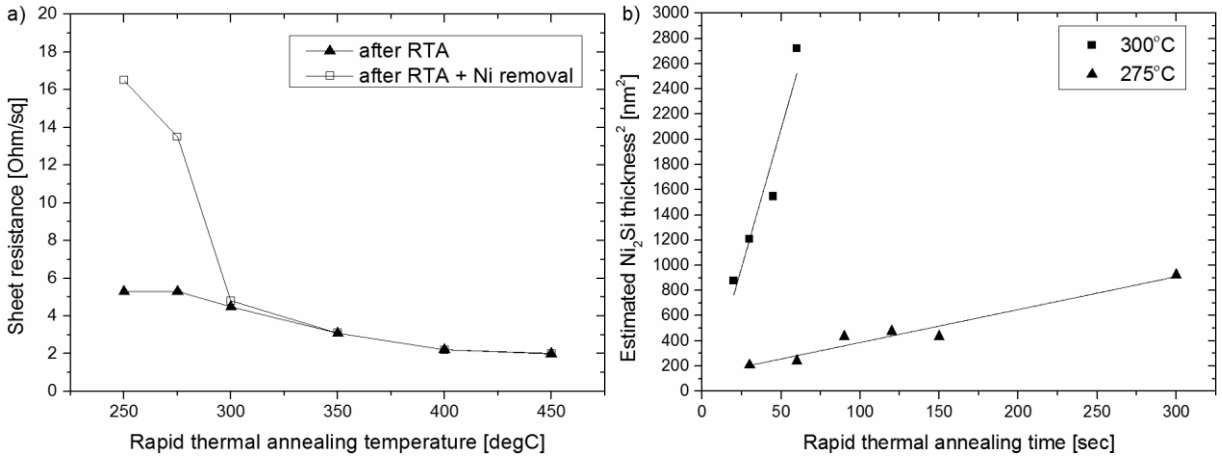


Figure 5.8: a) Sheet resistance of nickel silicides on alkaline textured 180 μm p-type CZ-Si as a function of rapid thermal annealing (RTA) temperature for 40 nm Ni. b) Square of estimated Ni_2Si thicknesses as a function of RTA time at 275˚C and at 300 ˚C on 180 μm p-type CZ-Si using 40 nm Ni.

In a next experiment, nickel silicide formation was evaluated on silicon solar cells devices. Large-area (12.5x12.5 cm^2) i-PERC type were manufactured on p-type Si, 1-2 Ω.cm, CZ-Si wafers according to the sequence given in Figure 5.1. However, contact formation was not based on a lift-off sequence as in the previous experiments. Self-aligned nickel silicide contacts were defined by patterning the front ARC, sputtering a thin (40 nm) Ni layer, performing a short rapid thermal annealing (30s at peak temperature), and removing unreacted Ni. Patterning of the front ARC was performed using the ns-UV laser ablation (LA) process developed earlier to form 20-30 μm wide line contacts (5 μJ/pulse, 75 KHz, 112.5 mm/s scanning speed). Photolithography patterning of the front ARC (20 μm wide contacts), using buffered HF, was used as control (WE samples). Finally, nickel silicides contacts were thickened by light-induced plating (LIP) of Ni (see Chapter 5.4) to achieve sufficient conductivity prior to Cu electroplating.

The influence of the RTA temperature was evaluated by measuring the pseudo Fill Factor (pFF) of the finished devices using Suns-Voc measurements. The pFF gives a good indication for junction damage. Low pFF values can be caused by shunting (i.e. metal spiking through the junction) or (local) increase in J_{02} recombination. In Figure 5.9a, it is shown that the pFF of LA cells degrades faster with increasing RTA temperature than for WE samples. Interestingly enough, the fact that the pFF of some LA cells drops below 80% already at 275°C cannot be explained by nickel silicide reaching the junction since the estimated Ni_2Si thickness at this temperature is below 40 nm (see Figure 5.8b) which is about 10x less than the junction depth. A continuous nickel silicide layer is obtained on WE samples annealed at 350˚C (Figure 5.8b). The nickel silicide layer is discontinuous for the LA samples annealed at 350˚C possibly due to non-uniform SiN_x removal (Figure 5.9c). In addition, ns-UV laser damage visible at the tips and edges of the pyramid could enhance nickel diffusion and explain the lower pFF values.

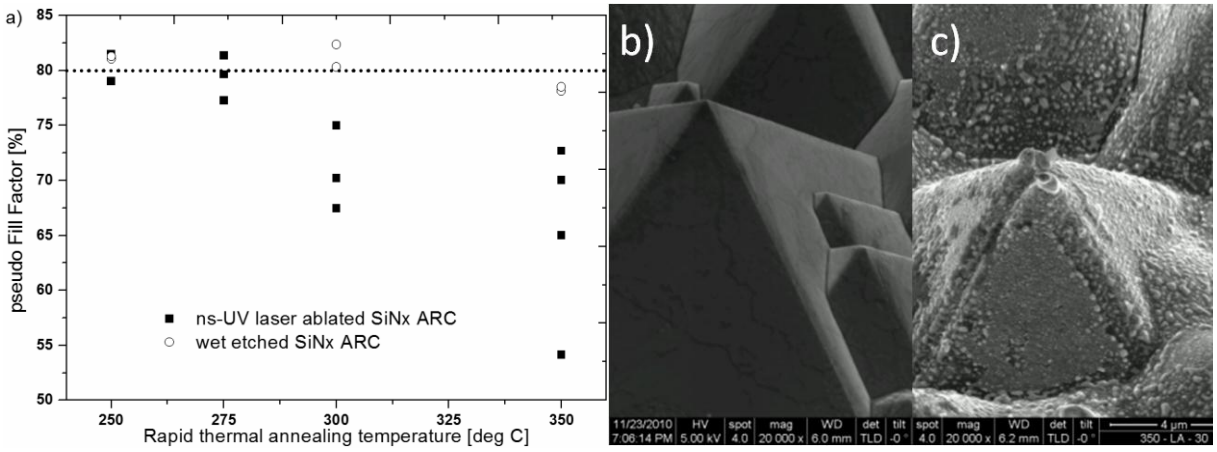


Figure 5.9: a) Pseudo Fill-Factor of 60 Ω/sq i-PERC cells with self-aligned Ni/Cu contacts as a function of nickel sintering temperature and for different SiN_x patterning methods. b) Scanning electron microscopy (SEM) image after unreacted Ni removal on a wet etched SiN_x. c) SEM image after unreacted Ni removal on ns-UV ablated SiN_x.

Transmission electron microscopy (TEM) analysis of the contacted areas were performed after unreacted Ni removal in an attempt to identify the mechanism(s) for junction degradation. In the case of 275°C annealing, sintering time was increased from 30s to 150s in order to get a sufficiently thick Ni_2Si layer to have good TEM image contrast. At 275°C a thin and uniform Ni_2Si layer is obtained along the pyramid walls of a WE sample (Figure 5.1a). The measured thicknesses, in the range of 40 to 50 nm, corresponds fairly well with the estimated values given in Figure 5.8b. Increasing the temperature to 350°C, part of the Ni_2Si layer is converted to NiSi (Figure 5.10b) which confirms the previous RBS measurements. The Si/NiSi interface roughness increases drastically. Despite the fact that the maximum silicide thickness measured in this TEM sample was around 100 nm, it is possible that the increase in interface roughness could be responsible for locally increasing J_{02} recombination particularly at valleys between pyramids where the junction depth is expected to be thinner than the measured 450 nm. As expected from the previous SEM images, a non-continuous nickel silicide layer is observed for the LA sample sintered at 350°C (Figure 5.10c). Surprisingly, Ni_2Si is locally formed on top of a thin amorphous a-SiN_x (~8 nm) which could indicate a case of "partial lift-off" since the a-SiN_x layer is much thinner than the original 80 nm ARC layer. Voids are detected in Si and could have been generated by the ns-UV laser ablation process or during sintering as reported by Foggiato et al. [FOG04]. Again, the silicide layer does not extend deep within Si and yet LA solar cells sintered at 350°C suffer from heavy junction damage. Though not visible in this TEM analysis, it is speculated from the SEM images (Figure 5.9c) that laser damage extends locally deeper. Crystal damage generated during laser ablation or voids could then serve as paths for enhanced diffusion of Ni and subsequent Ni clustering in the space charged region (j_{02} degradation) [TSU04].

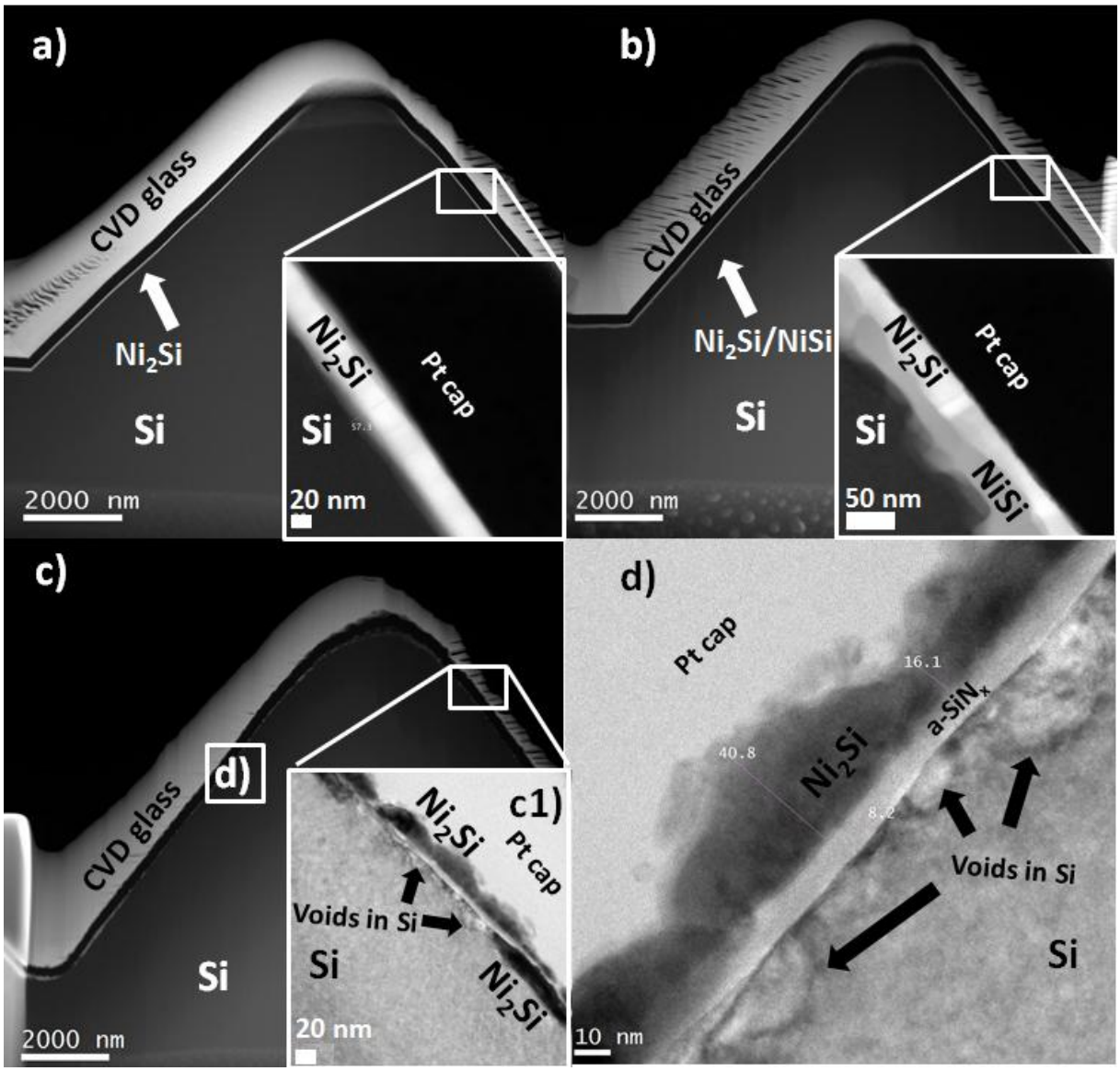


Figure 5.10: High-angle angular dark field (HAADF) transmission electron microscope (TEM) pictures of nickel silicide formed for: (a) after RTA at 275 ºC for 150s on wet etched (WE) ARC, (b) after RTA at 350 ºC for 30s on WE ARC, (c) after RTA at 350 ºC for 30s on ns-UV laser ablated (LA) ARC. For sample (c), further scanning TEM (STEM) analysis shown in in (c1) and (d) revealed Ni_2Si formation on top of the thin (~8 nm) remaining a-SiN_x layer as well as the presence of voids in Si. In all cases unreacted Ni was removed. Nickel silicide phases were determined by energy dispersive X-ray spectroscopy (EDS).

Apart from the two-step RTA which is seen as too complex for silicon solar cells, this analysis leads to the same recommendations as in the IC industry to minimize junction damage. These recommendations are (i) reduce RTA temperature and (ii) reduce deposited Ni thickness. It is also speculated that even though silicide thickness is kept below 50 nm and junction depth is around 450 nm, defects generated during ns-UV laser ablation on alkaline textured surfaces can lead to junction degradation. Therefore, additional recommendations include minimizing laser-induced damage and using deeper junctions.

The use of a deeper junction was investigated by modifying the starting $POCl_3$ diffusion profile and introducing a short thermal oxidation step (975˚C, 1 hour) after the PSG removal step (see Figure 5.1) to form a high-ohmic 120 Ω/sq deep emitter. During oxidation, dopants are driven-in deeper in Si. The junction depth increases from ~450 nm for the standard 60 Ω/sq emitter to ~600 nm. Consequently, the surface concentration (N_s) decreases from ~$2x10^{20}$ cm^{-3} down to ~$6x10^{19}$ cm^{-3}. The SiN_x thickness on top of the thin (~20 nm) thermal oxide (SiO_2) was adapted to keep the minimum reflectance at ~600 nm. Finally, a new grid design with fingers closer together (pitch=1 mm) was implemented to account for the increased emitter resistance. The same parameters were used for ns-UV laser ablation of the SiO_2/SiN_x double layer ARC. Self-aligned nickel silicides were formed by 40 nm PVD Ni, RTA (275˚C, 30s), unreacted Ni removal, LIP Ni plating, and Cu electroplating. These samples were benchmarked against self-aligned nickel silicides contacts formed by wet-etch patterning and to Ti/Cu defined by lift-off.

From the illuminated I-V results given in Table 5.2, self-aligned nickel silicide contacts consistently delivered average efficiencies ~19.2% which are equivalent to the ones obtained with the reference high efficiency Ti/Cu lift-off process. Average pFF values around 82% were achieved with laser ablated samples which demonstrates the robustness of the deep 120 Ω/sq emitter to damage associated with laser ablation and nickel silicide formation. Comparable series resistance and consequently comparable fill factors were obtained for all three cell types which shows that sufficiently low specific contact resistance values can be obtained with Ni_2Si to a low N_s emitter. The best laser ablated solar cell gave a short-circuit density of 37.6 mA/cm^2, an open-circuit voltage of 650 mV, and a fill factor of 79.3% yielding an energy conversion efficiency of 19.4% on large area CZ-Si (A=148.6 cm^2).

Table 5.2: Average and best illuminated I-V parameters of large area (A=148.6 cm^2) p-type, CZ-Si, i-PERC solar cells featuring a deep 120 Ω/sq emitter and Cu plated contacts. Self-aligned lithography-free Ni_2Si/Cu contacts are formed by wet etch (WE) or by ns-UV laser ablation (LA) patterning of the front SiN_x layer.

Contact type		j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	pFF [%]	η [%]	r_s [Ω.cm^2]
Ti/Cu lift-off	Avg. (3 cells)	37.8±0.0	649.7±0.6	78.5±0.7	81.6±1.0	19.2±0.1	0.6±0.1
	Best cell	37.8	650.0	79.0	82.6	19.4	0.7
Ni_2Si/Ni/Cu WE	Avg. (3 cells)	37.5±0.3	648.6±1.1	78.1±1.2	81.9±0.4	19.0±0.5	0.7±0.1
	Best cell	37.8	649.8	79.1	82.3	19.4	0.6
Ni_2Si/Ni/Cu LA	Avg. (3 cells)	37.7±0.2	650.6±0.5	78.6±1.9	82.2±0.3	19.3±0.5	0.7±0.3
	Best cell	37.6	650.2	79.3	82.5	19.4	0.7

From the dark I-V measurements, given in Figure 5.11, performed on cells with a 60 Ω/sq or a 120 Ω/sq 0.6 µm deep emitter, we can confirm that the poor pFF value (pFF < 80%) observed with Ni_2Si/Ni/Cu contacts on a 60 Ω /sq emitter are caused by a local increase in J_{02} recombination. Looking at Figure 5.11a, both 60 Ω /sq cells (WE Ni_2Si/Ni/Cu and reference Ti/Cu contacts) show the same j_{01} and R_{shunt} values (discarding again the presence of linear shunts). However, an increase in J_{dark} is visible at mid-voltage values for the Ni_2Si/Ni/Cu cell

that cannot be directly explained by a higher J_{02} recombination in the standard two-diode model. Observing the local ideality factor (Figure 5.11b), a hump is visible at voltages values close to the maximum power point voltage (V_{mpp}~0.52V) which can be explained by adding a resistance-limited diode with a high J_{02} recombination to the two-diode model [MCI01] (see Chapter 2.1.3). Similar humps in the local ideality factor have been observed for non-optimized laser ablation parameters prior to nickel silicide contact formation [KRA08, ALE09] and have been shown to be reduced by using deeper junctions below the contacts [MCI01]. This is confirmed in Figure 5.11d, where the local hump in local ideality factor at voltage values close to V_{mpp} is absent for both Ti/Cu and LA Ni_2Si/Ni/Cu cells featuring a homogeneous 120 Ω/sq deep emitter.

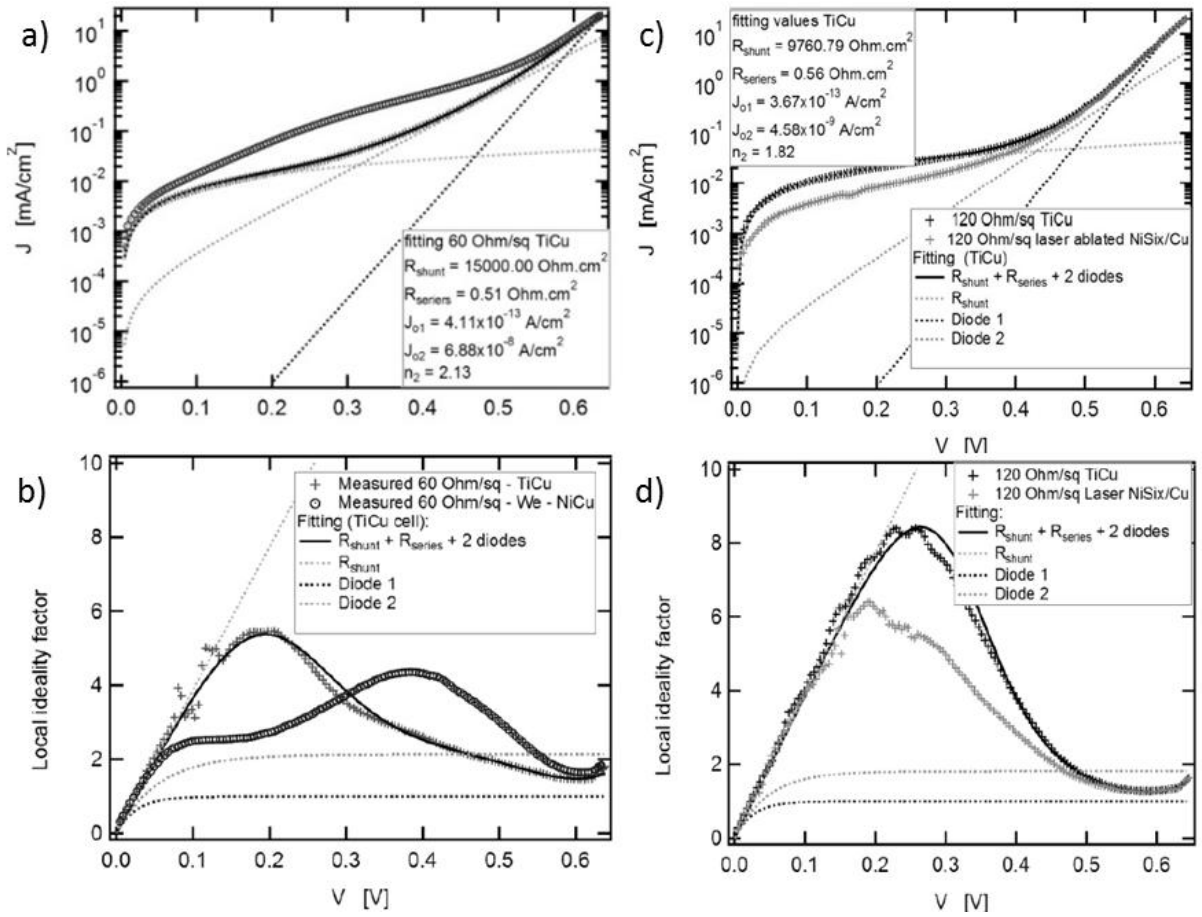


Figure 5.11: (a) Dark I-V measurements of 60 Ω /sq cells with wet etched Ni_2Si/Ni/Cu and lift-off Ti/Cu contacts. (b) Local ideality factors of the cells in (a). (c) Dark I-V measurements of 120 Ω/sq cells with laser ablated Ni_2Si/Ni/Cu and lift-off Ti/Cu contacts. (d) Local ideality factors of the cells of the cells in (c).

5.2.3. Contact resistance evaluation of nickel silicide contacts

To further evaluate the potential of Ni_2Si/Ni/Cu to contact low N_s high efficiency emitters, we designed an experiment where the emitter profile is grown by chemical vapor deposition (CVD) which allowed to control surface concentration and junction depth separately.

We used p-type, CZ-Si(100), mirror polished, 1-3 Ω.cm wafers. Wafers were cleaned in a H_2SO_4:H_2O_2 solution, rinsed in de-ionized water (DIW), dipped in 1% HF, and rinsed in DIW. Next the wafers were loaded in an Epsilon tool, a single wafer batch CVD system from ASM, and phosphorous doped emitters were grown with N_s targets of $1x10^{18}$, $5x10^{18}$, $1x10^{19}$, and $5x10^{19}$ cm^{-3}. The junction depth was chosen so that all emitters are about 80 Ω/sq. Spreading resistance profiling (SRP) results of three of the CVD profiles are shown in Figure 5.12a.

Specific test structures were then fabricated to evaluate the influence of Ns on the specific contact resistance (ρ_c) of different contact metals. Using PECVD silicon nitride deposited on the front side as a hard mask, the emitter was removed in a solution consisting of HNO_3:HF:CH_3COOH (1:1:8) to define mesas for ρ_c measurements based on the transfer length method (TLM, see appendix A). This was followed by a second photolithography step, aligned to the first one, to define TLM contact patterns by metal (Ti or Ni) lift-off. Finally, Ni was sintered at 275˚C to form Ni_2Si. From the ρ_c results, given in Figure 5.12b, it can be seen that Ni_2Si yields slightly lower ρ_c values than Ti or Ni at $N_s=2x10^{19}$ at/cm^3. The $8.4x10^{-4}$ Ω.cm^2 value obtained is quite close to the target $5x10^{-4}$ Ω.cm^2 value defined in Chapter 4. Increasing the temperature to above 400˚C to form NiSi did lead to lower ρ_c values. The present TLM structure might not be accurate enough to measure ρ_c values as low as the $5x10^{-6}$ Ω.cm^2 reported for the same N_s with NiSi by Stavistki [STA09]. For N_s values well below $1x10^{19}$ at/cm^3, Ni nor Ni_2Si do not appear to offer sufficiently low contact resistance values.

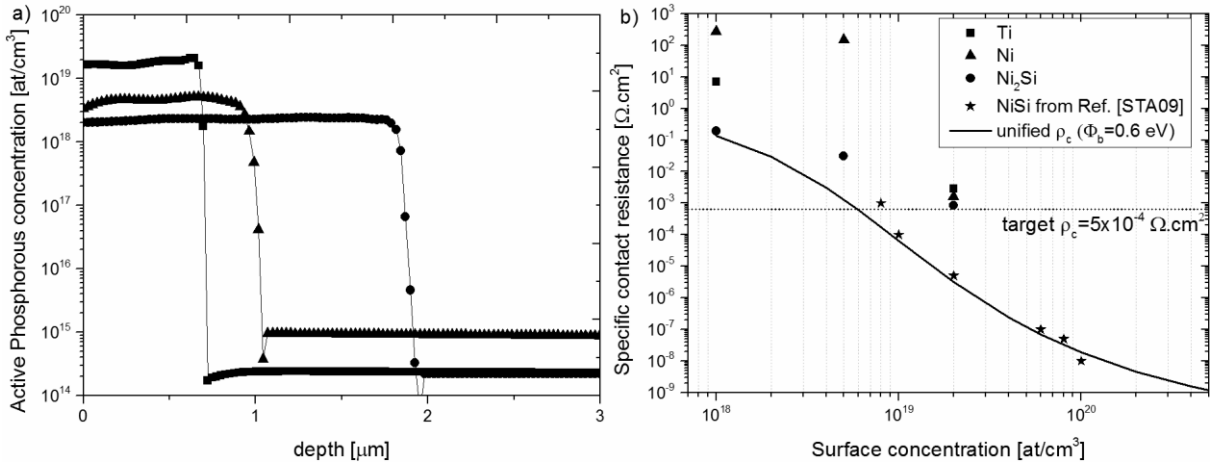


Figure 5.12: (a) Active Phosphorous concentration (determined by Spreading Resistance Probe (SRP)) of various n^+ profiles grown by epitaxy on Si(100). (b) Specific contact resistance (ρ_c) determined by the transfer length method for Ni, Ti, and Ni_2Si, ρ_c data for NiSi determined by Kelvin cross-bridge measurements [STA09] and ρ_c data computed using a unified model (barrier height=0.6eV) [THI13] are given for comparison.

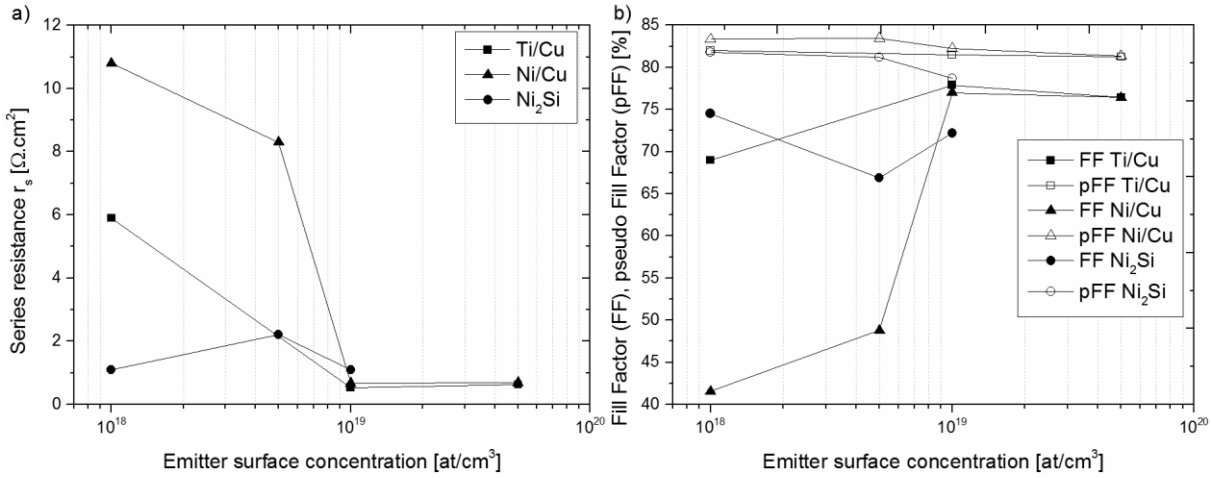


Figure 5.13: (a) Series-resistance determined by two-light level measurements [BOW01] for planar solar cells featuring a 80 Ω/sq epitaxial emitter with various surface concentrations (see Figure 5.12a) and various contact metals. (b) Fill Factor (FF) and pseudo Fill Factor (pFF) of the same solar cells as in (a).

The fact that emitters with different N_s all feature the same sheet resistance (80 Ω/sq) presents the advantage that the impact of contact resistance can directly be evaluated at cell level from the series resistance (r_s) since all other series resistance contributions (emitter resistance, line resistance, etc.) are in theory identical. This was done by processing further separate wafers into i-PERC solar cells and using lift-off to define the front H-pattern (40 µm wide contacts). It should be mentioned that the wafers with Ni_2Si contacts did not have any Cu or LIP Ni seed layer and hence suffered from non-uniform Cu plating leading to lower fill factors values. From the results given in Figure 5.13, it is shown that the increase in ρ_c observed for $N_s<1x10^{19}$ at/cm^3 leads to a drastic increase in series resistance and consequently to a large drop in fill factor. Therefore, homogeneous n^+ emitters should be tailored so that N_s is kept above $1x10^{19}$ at/cm^3.

5.3. Evaluation of electroless Ni seed layers

This section addresses electroless nickel deposition as an alternative to sputtering/evaporation since it presents the advantage of being a non-vacuum technique and enables selective nickel deposition (material waste). After shortly introducing background knowledge, the properties of two commercial electroless Ni baths are discussed and silicidation results are compared to silicidation results of pure sputtered Ni layers. More extensive evaluations of electroless Ni for the metallization of solar cells can be found in technical literature [KAR10, BOU12, ALE13]. Particularly valuable is the summary table for several commercial electroless baths given by Bartsch in his thesis [BAR12]. Books describing electroless plating fundamentals are also of particular interest [RIE91, MAL90, KAN07].

5.3.1. Background on electroless Ni deposition

In electroless plating, deposition is achieved using a reducing agent present in the electrolyte which provides the electrons to reduce metal ions at the silicon surface. Electroless

nickel deposition was first employed as a diffusion barrier for copper-plated contacts on silicon solar cells in the early 1980s and gained importance with the development of the LGBC concept in the late 1980s (see Chapter 3.2.7). In theory, self-aligned nickel deposits with good thickness uniformity can be obtained since deposition only occurs at the exposed silicon areas and the current distribution is very homogeneous (no external currents or fields are required).

Electroless nickel baths are mainly composed of: a metal salt (e.g. nickel sulphate, nickel chloride, nickel acetate) which contains the nickel cations to be deposited, a reducing agent which provides the electrons for the autocatalytic deposition, and a pH buffer to maintain the pH in the desired range. Ammonia (NH_3) and ammonium hydroxide (NH_4OH) are commonly used for pH control in alkaline solutions while hydrochloric (HCL) and sulfuric acid (H_2SO_4) are used in acidic solutions. The most common reducing agent is sodium hypophosphite (NaH_2PO_2) which leads to some degree of phosphorous (P) incorporation in the Ni layers (also called NiP layers). Alkaline baths typically have 5 to 10 atomic percent of P while acidic baths contain 10-30% [ABR94]. Other reducing agents which incorporate boron exist but they are not very common [MAL90, KAR10]. Commercial solutions also generally contain complexing agents, stabilizers, wetting agents, and other types of additives in order to improve the bath lifetime and the properties of the deposits. Complexing agents form Ni complexes which lowers the concentration of nickel cations in the electrolyte and hence prevent Ni precipitation. Stabilizers attach to metal seeds in suspension to prevent bath decomposition. Wetting agents reduce the surface tension of the surface to be plated to improve plating uniformity.

Electroless nickel deposition using hypophosphite as a reducing agent is commonly described by simultaneous cathodic and anodic reactions (mixed-potential theory [MAL90]) leading to the following summary equation:

$$Ni^{2+} + 2H_2PO_2^- + 2H_2O \xrightarrow{catalytic} Ni^0 + 2H_2PO_3^- + 2H^+ + H_2 \qquad (5.1)$$

However, this simplified reaction does not take into consideration all competing reactions occurring during NiP deposition. In particular, it does not explain the observed incorporation of phosphorous or oxygen in the layers . Different mechanisms have been proposed to account for these reactions and a summary is given by Aleman in her thesis [ALE13]. The difficulty for electroless deposition on silicon is that many factors complicate the deposition mechanisms. For instance, an Helmholtz double layer forms at the Si-electrolyte interface (see Chapter 2.2) and affects the transport of $Ni^{2+}$and $H_2PO_2^-$ species. Complexing agents alter the chemical properties of ions (e.g. the addition of ammonia changes the color of the nickel electrolyte from green to blue due to amines complexes replacing water molecules in the solvation shell around Ni^{2+}) [MAL90]. Silicon surface states which play an important role in charge transfer are affected by surface preparation (e.g. laser ablation, emitter doping, pre-clean) and by pH.

The properties of electroless nickel deposits generally differ whether they are obtained from acidic or alkaline baths [BOU12, ALE13]. Alkaline baths are described in literature as being more reactive which allows the use of lower deposition temperatures (40-80˚C) with the benefit of reduced evaporation and hence improved pH control. Alkaline NiP deposits typically

exhibit smaller grain size and better surface coverage that their acidic counterparts. For both alkaline and acidic NiP deposits, linear plating rates have been reported after a nucleation time. Nucleation time lowers while plating rate increases with temperature and pH.

Finally, the possibility of exposing solar cells shortly to light (<3 sec.) while immersing them into an alkaline bath was evaluated extensively by Boulord [BOU12] and Aleman [ALE13]. Reduced junction damage upon sintering were achieved with this technique, also called light assisted electroless process (LAEP), and were attributed to the ability to deposit thin (thickness <100 nm) with improved thickness control over conventional electroless.

5.3.2. Characterization of electroless Ni seed layers

Electroless nickel seed layers were evaluated as an alternative to PVD Ni layers with the objective of depositing thin (< 100 nm), uniform, and well adhering NiP layers prior to sintering.

Two electroless nickel baths, the composition and operating conditions of which are given in table 5.3, were used for preliminary evaluations on $POCl_3$ diffused (60 Ω/sq) polished and alkaline textured p-type Si(100) wafers. Since pre-cleaning was observed to yield improved uniformity as compared to a simple native oxide removal in 1% HF, test wafers were pre-cleaned in a Piranha solution (H_2SO_4:H_2O_2 followed by DIW rinse, 1% HF, and DIW rinse). Particular care was taken to shortly rinse the wafers in clean DI water since metal contaminated water promotes rapid oxidation of Si which hinders uniform NiP deposition. For the acidic bath, an additional surface activation step in Pd/HF/HCl for 5 seconds was required prior to deposition to achieve uniform deposits. Palladium ions are randomly reduced on silicon by galvanic displacement. Palladium makes the surface more catalytic which promotes NiP deposition.

Table 5.3: Acidic and alkaline electroless Ni baths composition and operating conditions. Both baths are based on semi-bright electroless Ni from Rohm and Haas (Ronamax SMT).

	unit	Acidic	Alkaline
Ni	[g/l]	6	6
Sodium Hypophosphite (NaH_2PO_2)	[g/l]	30	30
Deposition temperature	[˚C]	85	50
pH		5	10
Ammonium Chloride (NH_4Cl)	[g/l]	-	12.5
Ammonium Hydroxide (NH_4OH)	[ml/l]	-	100

As previously reported by Boulord and coworkers [BOU09], improved surface coverage is obtained for electroless Ni deposition at high pH. At low pH (pH=5, Figure 5.14a) the grain size is in the order of several microns while at high pH value (pH=10, Figure 5.14b) this value is reduced to some tens of nanometers. An important reason for this is the fact that the grain size of the metal can be tuned by the OH^- concentrations since the hydroxyl ion acts as a capping agent [SCH09]. Small NiP grain sizes ensure a large contact area between the metal and the semiconductor which is a prerequisite for good adhesion.

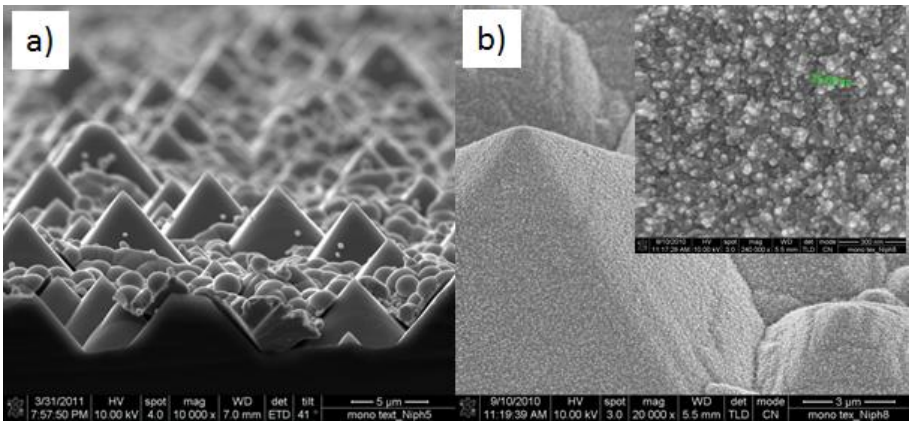


Figure 5.14: (a) Electroless Ni deposited at pH=5, T=85˚C. b) Electroless Ni deposited at pH=10, T=50 ˚C. The inset shows a close up of the layer, scale bar is 300 nm.

Based on the SEM analysis, the grain size is estimated to be ~25 nm at high pH (see inset). Based on RBS analysis performed on polished samples, the phosphorous content in the NiP layers was determined at 21% and at 6% for the acidic and alkaline baths respectively which corresponds reasonably well with literature data [ABR94]. The oxygen content in the alkaline NiP layers was found close to 10% based on elastic recoil detection (ERD). This is not surprising as phosphorous originates from the reducing agent present in the bath and a high pH value could promote the formation of metal (hydr)oxides.

Investigations were pursued with the alkaline bath. The sheet resistance was measured as function of deposition time at 50˚C (Figure. 5.15a). The resistivity value of 43.0 μΩ.cm (as compared to 11.7 μΩ.cm for PVD Ni) obtained from RBS was used to calculate the deposit thickness. During the first 15 seconds no deposition is observed which is possibly related to layer nucleation. The deposited thickness then increases linearly with time (deposition rate ~80 nm/min). Good adhesion (tape test) is achieved for layers up to 350 nm while larger thicknesses result in too much stress in the NiP film causing the layer to peel off.

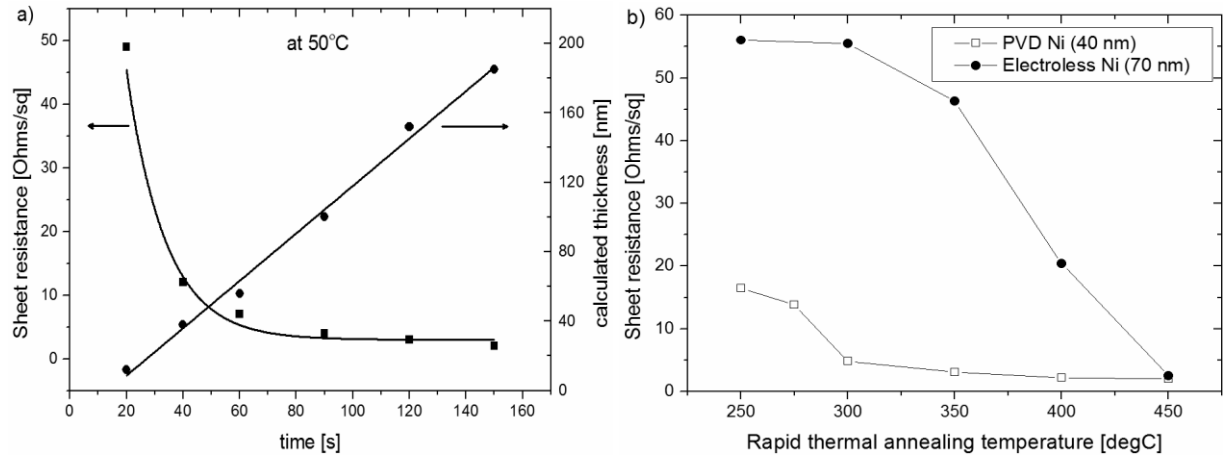


Figure 5.15: (a) Measured sheet resistance (R_{sh}) and calculated thickness of the NiP layer as a function of deposition time (T=50˚C). (b) Sheet resistance as function of sintering temperature after unreacted Ni removal in diluted SPM.

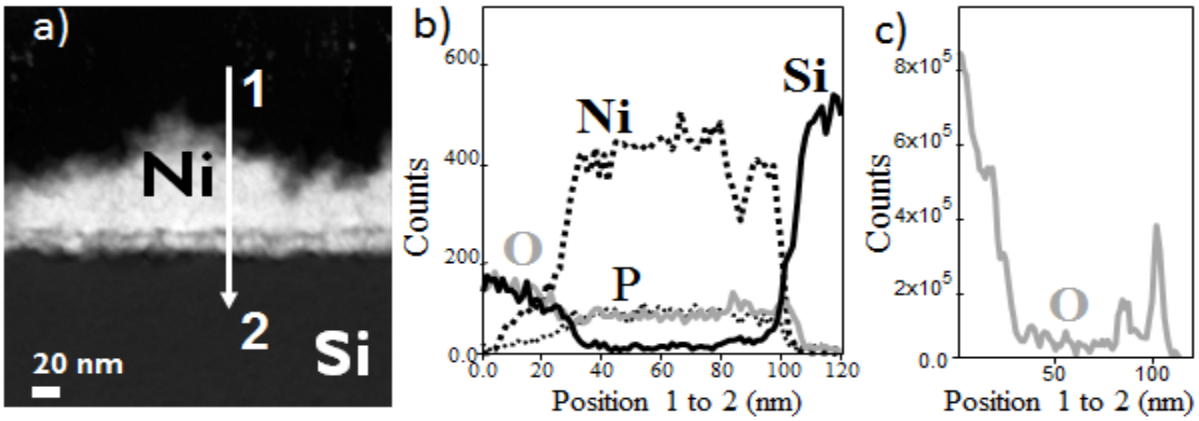


Figure 5.16: (a) Cross-section HAADF-STEM picture of a NiP layer (pH=10), black contrast indicates the presence of O, (b) EDS depth analysis, (c) Electron Energy Loss Spectroscopy (EELS) depth analysis.

The sintering temperature dependence of the sheet resistance, after unreacted Ni removal, obtained for a 40 nm sputtered Ni layer and a ~70 nm alkaline electroless NiP layer are shown in Figure 5.15b. In the case of the electroless NiP layer, the drop in sheet resistance occurs at much higher sintering temperature. Since nickel silicidation is a diffusion-limited process (see Chapter 5.2.2), both P and O present in the bulk NiP layer and especially at the interface (see below) could affect the silicidation either by delaying the supply of Ni atoms or by forming higher resistive metallic phases. Another important factor is the difference in thicknesses between the two layers which could cause a delay in silicidation due to the higher thermal absorption of the thicker layer (in this case electroless Ni).

In Figure 5.16a, a cross-section HAADF-STEM image is shown of an alkaline electroless NiP layer deposited on a mirror polished Si(100) substrate. It is clear that the layer thickness is not uniform and varies between 40 and 90 nm. The interface between the Ni layer and the Si substrate has roughened during the deposition process. The grain size is estimated to be 10 nm and is a more accurate approximation than the value obtained by SEM. The Ni deposit seems to consist of two layers, a ~20 nm layer at the bottom with a thicker layer on top. Since in HAADF-STEM heavier elements are visualized brighter than lighter ones, the dark contrast at the interface with Si and on top of the thin 20 nm NiP layer indicates the presence of oxygen. EDS analysis (Figure 5.16b) shows that phosphorous is incorporated uniformly in the layer and that Ni is present in both layers. With EDS it is difficult to determine the presence of oxygen due to a large background noise related to Ni. EELS analysis is, however, more sensitive and this measurement shows elevated oxygen levels in the bottom layer and two peaks, a larger one at the silicon/metal interface and a smaller one approximately 20 nm above the interface.

Alkaline electroless Ni deposition on silicon has previously been described as a two-step mechanism in which nucleation is followed by autocatalytic deposition involving the reducing hypophosphite ion. In the first step Ni is deposited onto the surface of the semiconductor via a charge transfer mechanism [REI07]:

$$Ni^{2+} + 2e^{-} \rightarrow Ni^{0} \qquad (5.2)$$

This process results in metal island formation and can be promoted by exposing the solar cell to light to create photo-generated carriers as mentioned in the previous section (5.3.1). Nickel in contact with Si creates a galvanic cell in which a mixed potential is established. On the metal side of the interface, Ni deposition is enhanced (equation 5.2) while on the semiconductor side galvanic oxidation is promoted which explains the oxide present at the interface:

$$Si + 4OH^- \rightarrow SiO_2 + 2H_2O + 4e^- \quad (5.3)$$

A silicon oxide as thick as 50 nm has been observed during this nucleation step [TAK00]. However, in our TEM analysis (Figure 5.16) we could not identify such thick oxide layers. A possible explanation is that, instead of forming solely SiO_2, significant galvanic etching of Si occurs at high pH producing a water-soluble complex which is released into the solution according to the overall redox equation [SEI90]:

$$Si + 6OH^- + 4h^+ \rightarrow [SiO_2(OH)_2]^{2-} + 2H_2O \quad (5.4)$$

Such galvanic etching of the semiconductor with a water-soluble complex would explain the observed surface roughening. A similar mechanism involving soluble silicates at high pH was also proposed by Boulord in her thesis [BOU12]. Equations (5.3) and (5.4) are influenced by the concentration of OH^-, which would explain the shorter nucleation times observed with higher pH [BOU12]. Once the nucleation layer is fully closed, galvanic interaction between the metal and the semiconductor no longer occurs and the autocatalytic Ni deposition takes over. First, the hypophosphite ion is decomposed at the metal surface to form a hydride:

$$H_2PO_2^- + H_2O \xrightarrow{catalytic} H_2PO_3^- + H^+ + H^- \quad (5.5)$$

In the next step the hydride reduces the Ni ion to the metallic state releasing hydrogen which marks the end of the nucleation step as observed experimentally:

$$2H^- + Ni^{2+} \xrightarrow{catalytic} Ni^0 + H_2 \quad (5.6)$$

In parallel, phosphorous is incorporated into the NiP layer according to the following reactions [HSU09]:

$$Ni^{2+} + H_2PO_2^- + 2H^+ + 3e^- \xrightarrow{catalytic} Ni - P + H_2O \quad (5.7)$$

$$H_2PO_2^- + 2H^+ + e^- \xrightarrow{catalytic} P + H_2O \quad (5.8)$$

It is speculated that the oxide detected on top of the nucleation layer is an induction time effect. The build-up of active species needs to be sufficient in order for the electroless reaction to become sufficiently fast. In the meantime oxidation of the metal occurs due to high pH.

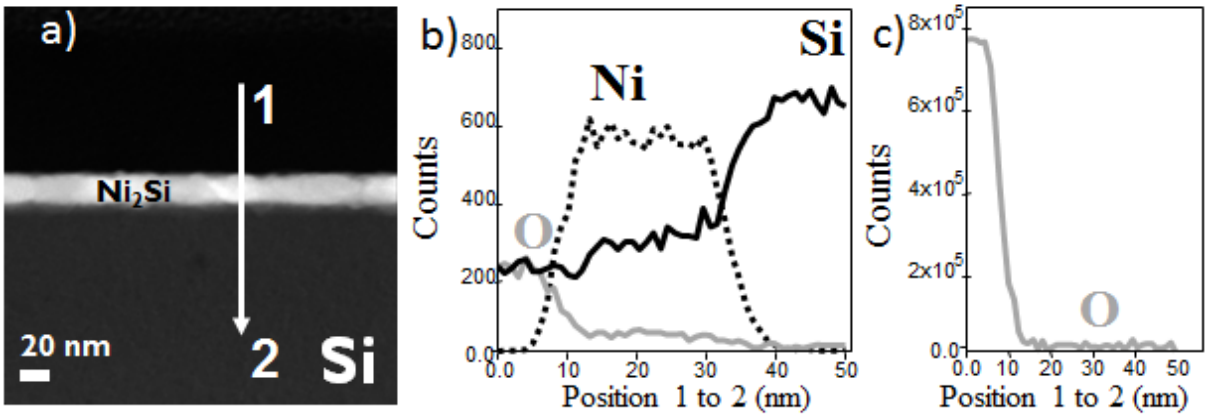


Figure 5.17: a) Cross-section HAADF-STEM picture of a NiP layer (pH=10) after sintering at 350˚C for 30 seconds, unreacted Ni was selectively removed in diluted SPM , (b) EDS depth analysis, (c) EELS depth analysis.

The silicide layer formed after an RTA step of 350ºC for 30s is thin, smooth and quite uniform in thickness (Figure 5.17a). The thickness varied between 18-28 nm. This variation in thickness is significantly less than that of the starting layer (Figure 5.16a). This might contradict the general assumption that silicide thickness is directly proportional to the deposited Ni thickness and hence that non-uniform electroless Ni deposits are responsible for higher leakage currents [BOU12, ALE13]. EDS quantification (Figure 5.17b) shows that the silicide formed consists of Ni_2Si. Additionally, no traces of P were found by EDS analysis and no oxide is detected by EELS (Figure 5.17c). As mentioned earlier in section 5.2, the nickel versus nickel silicide(s) selectively of SPM is based on the fact that oxidation and dissolution of unreacted Ni stops when a silicon oxide layer is formed on top of the silicide layers. Therefore, the presence of Ni_2P and/or Ni_3P phases that typically form upon sintering NiP layers [BOU09, DUH13] cannot be confirmed from this TEM/EDS analysis since such phases do not contain Si and hence would have been removed during the unreacted Ni etch step in diluted SPM that was performed prior to the measurement. Accumulation of P and O species in the unreacted Ni layer during annealing, as reported by Duhin et al. [DUH13], would also explain their absence in EDS/EELS results.

The kinetics of nickel silicide formation for PVD Ni and alkaline electroless Ni were studied by in-situ x-ray diffraction (XRD). In-situ XRD measurements were performed in a Bruker D8 Advance XRD setup using Cu Kα radiation (λ= 0.1540 nm). The results, given in Figure 5.18, confirm that nickel silicide formation occurs faster for the 40 nm PVD Ni than for a ~70 nm electroless NiP layer. Interestingly, there is a difference in the preferred orientation of Ni_2Si and NiSi phases from the NiP layer as compared to those obtained for the PVD Ni layer. The Ni_2Si layers obtained from NiP have the (321) preferred orientation while the layers obtained from PVD Ni were with (133) preferred orientation. The (200) NiSi peak at 34.6º that is strongly visible for layers obtained from NiP is absent for layers obtained from PVD Ni. These differences may be caused by the formation of the Ni_2P phase which occurred concurrently.

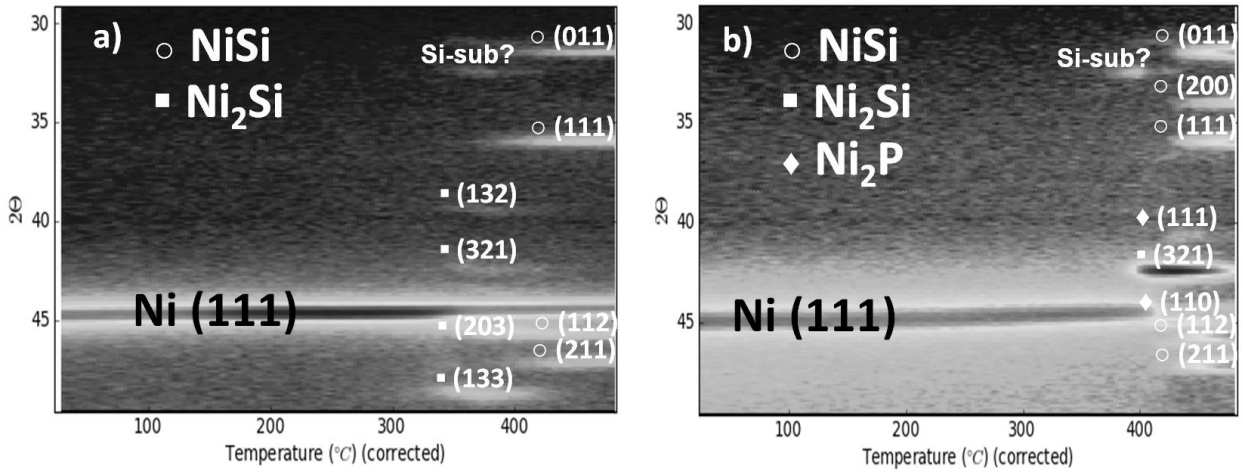


Figure 5.18: In-situ XRD measurements during temperature ramping (1 °C/s) for (a) 40 nm PVD Ni and (b) 70 nm alkaline electroless NiP layer. Polished p-type Si (100) substrates were used.

Although the initial alkaline electroless Ni layers were non-uniform, uniform Ni_2Si layers were formed with a smooth interface to Si and without significant P and O incorporation. Slower silicidation kinetics as compared to PVD Ni were also demonstrated which potentially reduces the risk of shunting the junction upon sintering. However, the higher sintering temperature that are required might also result in faster in-diffusion of Ni and subsequent Ni clustering in the space charged region (j_{02} degradation) [TSU04].

Despite these promising results, the use of electroless Ni seed layers was not further pursued. The main reason for this is the too small process window that was found in order to achieve sufficient pull tab adhesion and minimize diode damage on a 0.6 µm deep 120Ω/sq emitter (see Chapter 7). In addition, thick NiP layers (> 350 nm) that are required to achieve sufficient conductivity prior to Cu electroplating were found to be non-adherent and hence an additional light-induced plating of Ni (~1 µm) step had to be performed prior to Cu plating. Finally, the possibility to perform nickel silicide formation at the end of a simple LIP Ni + Cu plating sequence (see next section) made the current electroless process too complicated particularly when considering the poor lifetime of the electroless bath used in this study. Disadvantages of electroless seed layers are further discussed in section 5.5.

5.4. Evaluation of light induced plated Ni seed layers

In this section relative thick (~1 µm) Ni seed layers deposited by light-induced plating (LIP) are evaluated as an alternative to thin Ni layers deposited by sputtering/evaporation. After introducing background knowledge on LIP, the behavior of LIP of nickel on silicon is described. One of the key development in this work is presented, which allows to form nickel silicides after completion of the full Ni/Cu/Ag metal stack. Finally, the challenges associated with transferring this process to inline pilot production sintering and plating tools are discussed.

5.4.1. Background on light induced plating

Light-induced plating (LIP) can either be performed contactless ("non-contact LIP") or simply by contacting the rear side of the cell ("bias-assisted LIP") [LEN12].

Non-contact LIP was first described for the metallization of solar cells in a patent filed by Durkee [DUR79] and refers to the case where the cell being plated is not electrically contacted. The cell is fully immersed in the electrolyte containing metal ions. Upon illumination, electrons collected by the front n^+ emitter become available for metal reduction at the areas exposed to the electrolyte while holes drift to the rear surface (e.g. Aluminum (Al)) where they recombine with electrons generated by the oxidation of the rear electrode. Since oxidation of the rear-side is needed to sustain deposition at the front side, the use of corrosion agents (e.g. chloride or bromide ions) in the electrolyte is required in the particular case of Al since it forms a barrier oxide layer which blocks further corrosion [LEN12]. Alternatively, the rear electrode can be made of the metal (e.g. silver (Ag), copper, or nickel) to be deposited at the front.

Dissolution of the rear electrode can be prevented by connecting the rear side to a sacrificial metal anode immersed in the solution. However, if an effort is made to contact the rear side it becomes advantageous to apply a potential between the sacrificial anode and the rear side as first described by Grenon [GRE81]. Bias-assisted LIP presents the advantages that: (i) dissolution of the rear side can be prevented (i.e. cathodic protection), (ii) significantly faster plating rates can be obtained than with non-contact LIP, (iii) simultaneous plating on both sides can be obtained if desired. The faster plating rates are the result of the bias reducing the impedance of the circuit and enabling the plating current to operate closer to the short-circuit current generated by the cell in the electrolyte.

Over the recent years, significant progress were made in understanding the behavior of bias-assisted LIP on metal seed layers [MET07, BOU12, BAR12]. Investigations performed by Bartsch for bias-assisted LIP (schematic given in Figure 5.19a) of Ag on printed Ag seed layers were particularly insightful and key observations are given hereafter.

In the case of a covered rear side (or rear side not immersed in the electrolyte), process control is similar to electroplating since the deposited mass at the front side behaves proportionally to the plating current. The difference is that the plating current I_{LIP} , measured between the rear side of the cell and the anode, is controlled by the potential between the rear side and the auxiliary anode (Δ_{RS-AUX}). Increasing further Δ_{RS-AUX}, I_{LIP} becomes limited by the

current generated by the cell particularly at low light intensities as shown in Figure 5.19b. At that stage, the absolute potential of the front side only drops slightly and the potential difference between front and rear side (Δ_{FS-RS}) becomes zero or negative. However, this state is rather difficult to achieve for high irradiation intensities as the plating current becomes high and limited by the electrolyte [MET07]. A further increase in voltage does not result in faster plating rates until the potential for hydrogen formation (i.e. water decomposition) is reached leading to poor quality deposition (porous/burnt layer). Thus, the process is typically run in a region where the plating current is limited by Δ_{RS-AUX} and not by the electrolyte.

In the case where the solar cell is fully immersed in the electrolyte (open rear side), the current paths in bias-assisted LIP are more complex since oxidation/reduction reactions can occur at three electrodes (front side, rear side, auxiliary anode) which are interlinked. It was found that at high light intensities, the potential Δ_{FS-RS} is almost constant and equal to the cell voltage at maximum power point as shown in Figure 5.20a. In these cases, a higher protective potential (Δ_{RS-AUX}) increases the front side plating rate until it becomes limited by the cell photo-generated current or by the electrolyte (not shown in Figure 5.20a). Beyond a certain cathodic potential, plating starts to occur at both front and rear sides. The current I_{LIP} becomes the cumulative current between front side and anode, and rear side and anode. This effect is particularly important at low light intensities where the presence of shunts or edge effects become dominant. This is mirrored in Figure 5.19b, where I_{LIP} increases for higher protective potentials Δ_{RS-AUX} (i.e. lower Δ_{FS-RS}), due to plating on the open rear side of the solar cell.

In summary, not taking into account interface effects (i.e. Helmholtz double layer), bias-assisted LIP can be described by the simplified equivalent circuit given in Figure 5.20b.

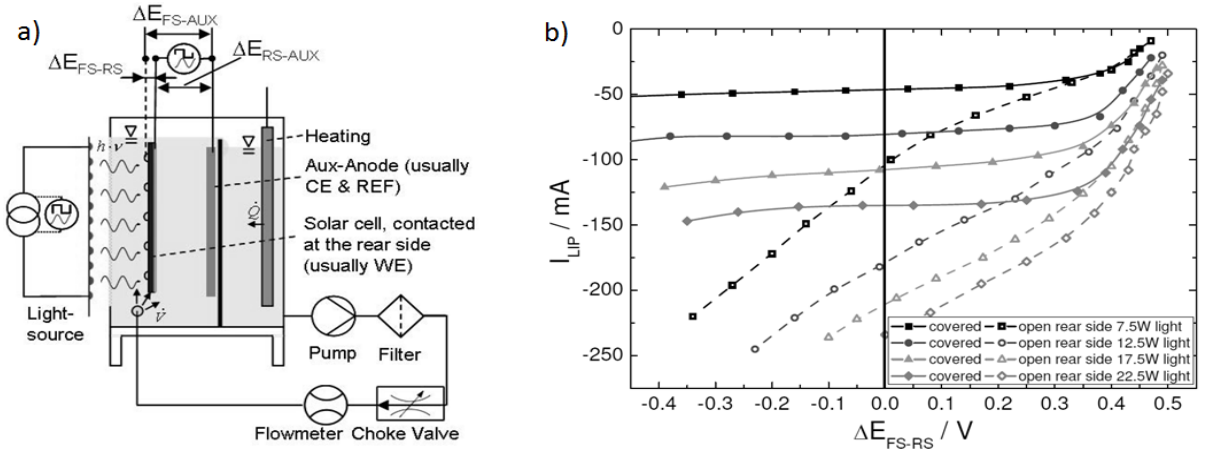


Figure 5.19: a) Schematic of bias-assisted LIP setup. Usually, a protective potential (Δ_{RS-AUX}) is applied between the rear side of the solar cell and the auxiliary (AUX) anode (e.g. Ni anode) which serves as counter (CE) and reference (REF) electrode. Ni deposition occurs at the front side (FS) as well as at open rear side (RS) of the solar cell, which serves as working electrode (WE), depending on Δ_{RS-AUX}. b) Behavior of I_{LIP} (between rear side and anode) versus potential between front side and rear side (Δ_{FS-RS}), for various light intensities, for a covered or an open rear side. Both figures are taken from [BAR12].

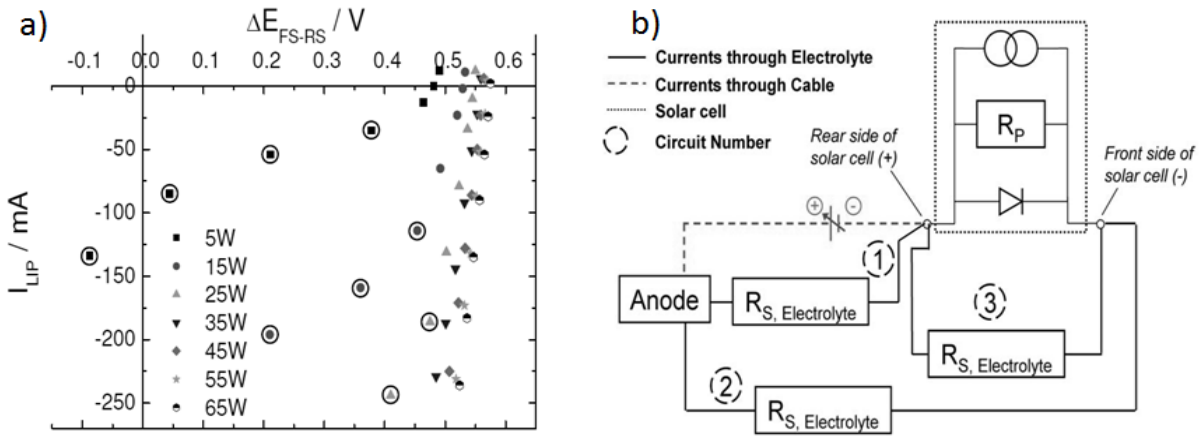


Figure 5.20: a) Relation between I_{LIP} (between rear side and anode) versus potential between solar cell front side and rear side (Δ_{FS-RS}) for various light intensities, b) Simplified equivalent circuit for bias-assisted LIP. Both figures are taken from [BAR12].

As mentioned by Lennon and coworkers [LEN12], many commercial bias-assisted LIP systems maintain the rear surface of the solar cells out of the electrolyte. As mentioned before, this eliminates the risks of plating on the rear side and/or of Al dissolution (particularly if Al is contact with Ag rear pads leading to galvanic corrosion of the surrounding Al since Ag is a more noble metal). Another reason for keeping the rear side "dry" is that in case of screen-printed Al, which is porous, the immersed Al layer might be difficult to totally dry and the retained moisture might affect the subsequent encapsulation process. However, keeping the rear side dry results in a more complex system and is difficult to mimic in a lab setup. Therefore, all bias-assisted LIP nickel investigations were performed by immersing the cells fully in the electrolyte and the process developed in this thesis was transferred to a simple commercial system where the cells are also fully immersed in the electrolyte.

5.4.2. Bias-assisted light induced plating of nickel on silicon

Bias-assisted LIP Ni on silicon requires to consider the case of semiconductor-electrolyte interface. As introduced in Chapter 2.2, the Fermi level for a n-type semiconductor (E_F=-4.05 eV) is typically higher than the redox potential of the LIP Ni electrolyte (E_0=-4.27 eV). Upon immersion in the electrolyte, the electrochemical potentials need to equalize and hence electrons will be transferred to the electrolyte leading to an upward band bending (see Figure 5.21a, $E>E_{FB}$). Applying an external potential shifts the Fermi levels and at certain applied potential, called flat-band potential (E_{FB}), the Fermi levels of the semiconductor and the electrolyte are equal (no transfer of charge, no band bending, see Figure 5.21a, $E=E_{FB}$). At potentials negative of this flat-band potential ($E< E_{FB}$), accumulation is obtained resulting in excess electrons at the surface (see Figure 5.21a, $E<E_{FB}$) and cathodic processes can occur via the conduction band.

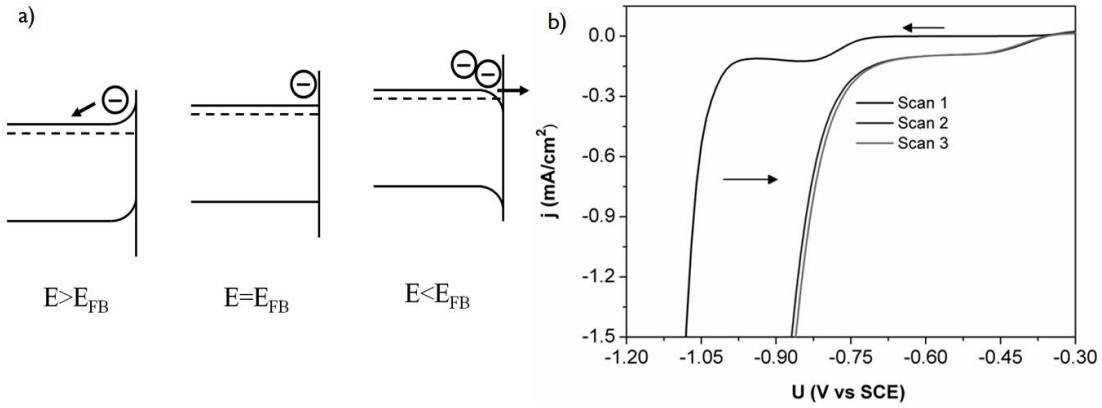


Figure 5.21: a) Energy band diagram of a n-type semiconductor-electrolyte system presenting a flat-band potential E_{FB} for various applied voltage E. b) Consecutive current density-potential scans of 2x2 cm^2 planar n-type Si(100) in a 0.62M sulphamate Ni plating solution (pH=3.9) in the dark. Applied potentials are given versus the saturated calomel electrode (SCE).

Electrochemical measurements were first performed on 2x2 cm^2, 9-15 Ω.cm, planar n-type Si(100) to develop basic understanding of electrochemical processes involved in the reduction of Ni on n-type Si. An electrical contact was provided by applying a gallium/indium eutectic on the scratched backside of the substrate. The sample was mounted in a sample holder on a Cu block to provide the Ohmic contact. The front side was selectively exposed to the Ni electrolyte (surface area 0.825 cm^2). The Ni plating solution was made up using a concentrate solution of Ni sulphamate (65% w/w, Rohm and Haas) and boric acid (Merck, p.a. grade). Concentration of both components in the bath amounted to 0.62 M and the pH was measured at 3.9. Prior to the electrochemical measurements, native oxide was removed in 1%HF for 1 minute followed by a short rinse in de-ionized water. For the electrochemical measurements, a three-electrode setup was used with the Si substrate as the working electrode, a Pt counter electrode and a saturated calomel electrode (SCE). All potentials are given with respect to SCE. Current potential plots were recorded with a PalmSens potentiostat at room temperature.

Figure 5.21b shows consecutive scans of current density-potential in the dark for a n-type Si(100) sample in the Ni plating solution. For negative potentials, two cathodic processes occur:

$$Ni^{2+} + 2e^- \rightarrow Ni \qquad (5.9)$$

$$2H_2O + 2e^- \rightarrow H_2 + 2OH^- \qquad (5.10)$$

At potential negative with respect to -0.70V, the current density increases due to the reduction of Ni (reaction (5.9)). This indicates that the flat-band potential is located at around -0.70V. As indicated by the formation of gas bubbles, water reduction, reaction (5.10), becomes important at potentials lower than -0.96V. However, after some Ni is deposited on the surface during the first scan, the onset for the reduction of Ni shifts towards a considerably more positive potential of -0.35V (scans 2 and 3, Figure 5.21b). Atomic force microscopy (AFM) measurements were performed on planar n-Si(100) for Ni layers deposited in the dark at -0.90V

vs. SCE and for various durations (10s, 30s, 60s). Ni nuclei densities were calculated from the AFM images and the results are given in Figure 5.22d. After a short nucleation period, the density of Ni nuclei saturates as they grow in size due to fact that Ni-on-Ni deposition is favored over Ni-on-Si. As with electroless solutions, several factors (pH, wetting agent, surface defect density, native oxide, etc.) possibly play an important role in the nuclei density.

Electrochemical measurements were then performed on 4*4 cm^2 solar cells laser diced from 12.5x12.5cm^2 p-type full Al-BSF solar cells featuring a 60 Ω/sq $POCl_3$ emitter. Contacts openings were made in the front SiN_x by ps-UV laser ablation, exposing the emitter to the electrolyte. The front side and backside were selectively exposed to the electrolyte; shunting effects on the edges of the sample were excluded using chemical resistant tape. The electrical contact was not in contact with the electrolyte. For each measurement, a fresh sample was used. Bias-assisted LIP Ni was done in a rectangular glass beaker using the abovementioned chemistry and sample pretreatment for native oxide removal. A green LED panel (5x6 lamps) was mounted on the outside of the beaker. A large area platinized titanium mesh anode was positioned in between the LED source and the sample to ensure homogeneous illumination and electric field distribution during deposition. Samples were placed at ~5 cm away from the LED panel. Measurements were performed at various light intensities by varying the drive current as the light intensity was shown to scale linearly with it (see Chapter 9).

The band energy diagram for a p-type Al-BSF solar cell is shown in Figure 5.23a. As shown in this schematic, the presence of the space charged region can separate photo-generated carriers leading to an accumulation of electrons at the surface and hence Ni plating even without the application of an external voltage (i.e. non-contact LIP with dissolution of rear Al to maintain plating). Also shown in this schematic is the fact that the potential of the backside is more positive than the one of front side. Unsurprisingly, the onset for Ni reduction at the backside is found at more cathodic potentials than for Ni reduction at the front side as shown in Figure 5.23b. Increasing the light intensity, the concentration of electrons available at the surface increases and the Ni plating onset lowers from -0.75V to -0.6V. The current density increases with increasing cathodic potentials and hence higher plating rates or simultaneous plating at both sides can be achieved with bias-assisted LIP.

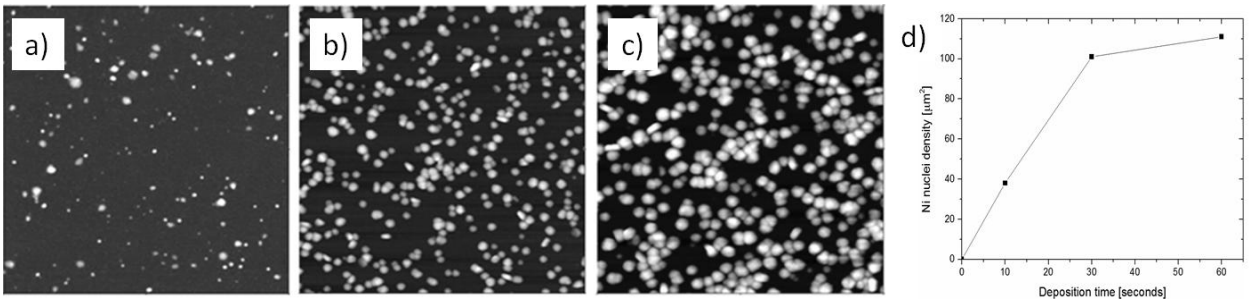


Figure 5.22: Atomic force microscopy (AFM) images of 2x2 μm^2 n-type Si(100) for Ni deposition time (a: 10s, b: 30s, c: 60s) at -0.90V vs. SCE in the dark. d) Ni nuclei density vs. deposition time obtained from AFM images.

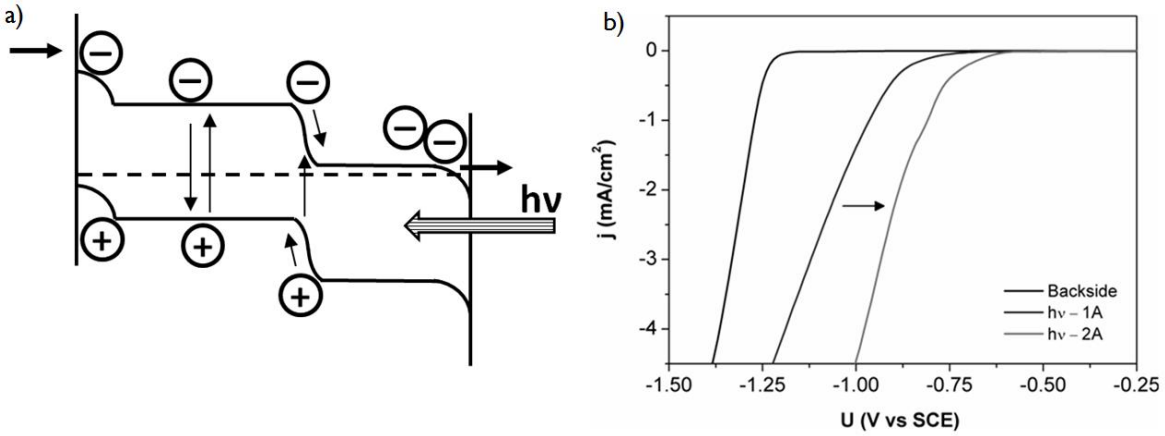


Figure 5.23: a) Energy band diagram of Al-BSF p-type solar cell under illumination. b) Current density-potential plots of 4x4 cm^2 Al-BSF p-type solar cells in a 0.62M sulphamate Ni plating solution (pH=3.9) at room temperature. The backside or the front side (at various light intensities) are selectively exposed to the plating solution using chemical resistance tape to protect the opposite side and the sample edges. New samples are used for each scan. Potentials are given versus the saturated calomel electrode (SCE).

We have demonstrated for Ni plating in the dark that Ni-on-Ni deposition is favored over Ni-on-Si and that it leads to Ni nuclei growth rather than to an increase in Ni nuclei density. The application of light increases the electron concentration at the surface and hence could potentially favor a more uniform Ni nucleation. Looking at scanning electron microscope images of bias-assisted LIP Ni on ps-UV ablated surfaces, we find that Ni nucleation occurs preferentially at some locations (see Figure 5.24a) and that longer deposition times (or higher applied voltages) lead to Ni nuclei growth (see Figure 5.24b). Uniform ps-UV laser ablation of dielectric(s) on alkaline textured surfaces is problematic (see Chapter 6.2.4). Some areas present more surface defects which possibly favor Ni nuclei formation while others are covered with dielectrics(s) blocking Ni deposition. As a result, uniform coverage of thin (<100 nm) Ni layers by LIP (non-contact LIP or bias-assisted LIP) is challenging and the deposition of closed layers requires thick deposits as shown in Figure 5.24d. The deposition of thin layers together with the influence of several bias-assisted LIP Ni process parameters (electrolyte temperature, light intensity, applied voltage, etc.) is addressed in Chapter 9.

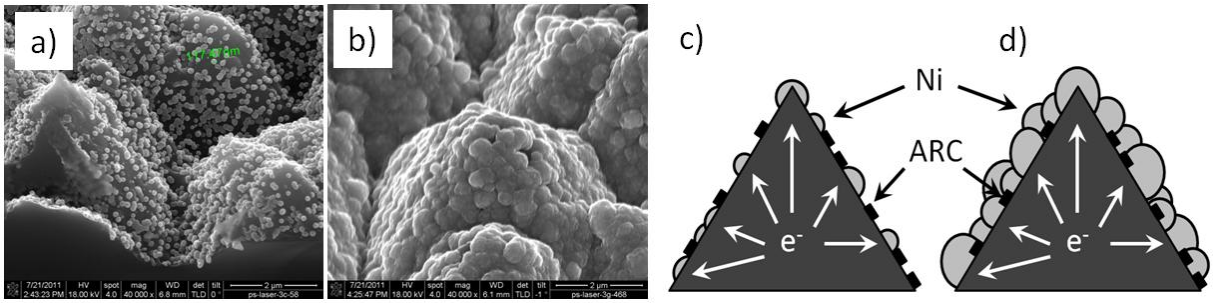


Figure 5.24: Scanning electron microscope images of bias-assisted LIP Ni plating (Δ_{RS-AUX}=-0.2V, LED drive current=1A) of ps-UV ablated alkaline textured surfaces after a) 60s and b) 470s. Schematic of LIP Ni plating on laser ablated alkaline textured surfaces after nucleation (c) and layer growth (d).

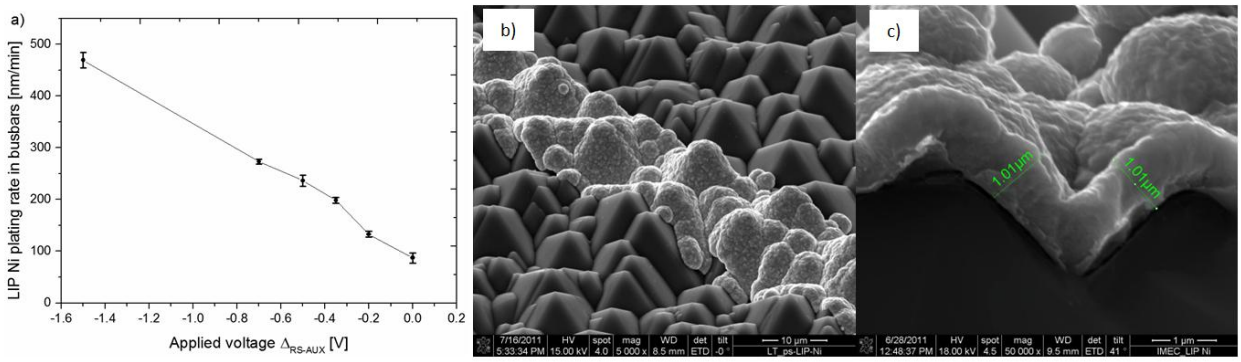


Figure 5.25: a) Bias-assisted LIP Ni plating rate in busbars areas at various protective potentials (Δ_{RS-AUX}). This graph is further discussed in Chapter 9. b) and c) Scanning electron microscope images of thick (~1 µm) Ni layers.

The fact that fast plating rates (>200 nm/min) can be obtained by bias-assisted LIP Ni is demonstrated in Figure 5.25a. Such plating rates enable the deposition of relatively thick (~1 um) and uniform self-aligned Ni layers in less than 4 min as shown in Figure 5.25b and c. Such layers have been used to increase conductivity of PVD Ni or electroless NiP seed layers prior to Cu-electroplating and can be used to form self-aligned nickel silicides contacts as discussed next.

5.4.3. Development of a simplified plating sequence

So far, the nickel silicidation step was performed after deposition of a thin (<100 nm) Ni seed layer (PVD Ni or electroless NiP). An extra Ni thickening step was found to be required prior to Cu-electroplating in order to achieve sufficient conductivity and hence uniform plating. Alternatives such as electroless Cu (as originally used by BP Solar, see Chapter 3.2) or LIP-Cu which are compatible with thin Ni layers do exist. However, thin Ni layers might fail faster than thick layers since Ni acts as sacrificial barrier to Cu diffusion (the impact of Ni thickness on Cu diffusion is further discussed in Chapter 7). We have shown that electroless deposition is relatively slow (deposition rate ~80 nm/min) and that thick electroless Ni layers (>350 nm) tend to be non-adherent. We have just demonstrated that bias-assisted LIP Ni enables the deposition of thick, adherent Ni layers relatively quickly (deposition rate ~200nm/min). Based on these considerations, we chose to use a bias-assisted LIP Ni thickening step prior to Cu-electroplating.

It would be advantageous if silicidation could be performed using only the thick (~1 µm) bias-assisted LIP Ni layer (meaning removing the PVD Ni or electroless NiP deposition step). It would be even more advantageous to perform the silicidation step after completion of the full Ni/Cu/Ag metal stack as shown in Figure 5.26. This is because, by performing the silicidation step at the end, only one surface activation (HF clean) is required and all metal layers can be deposited in a single plating system. The need for a second surface activation step in the case where silicidation is performed after Ni deposition is demonstrated in Chapter 7. Despite being the simplest plating sequence, sintering at the end potentially suffers from risks of Cu-diffusion and limits the solderable capping layer to the use of Ag due to the low melting point (~232˚C) of tin (Sn).

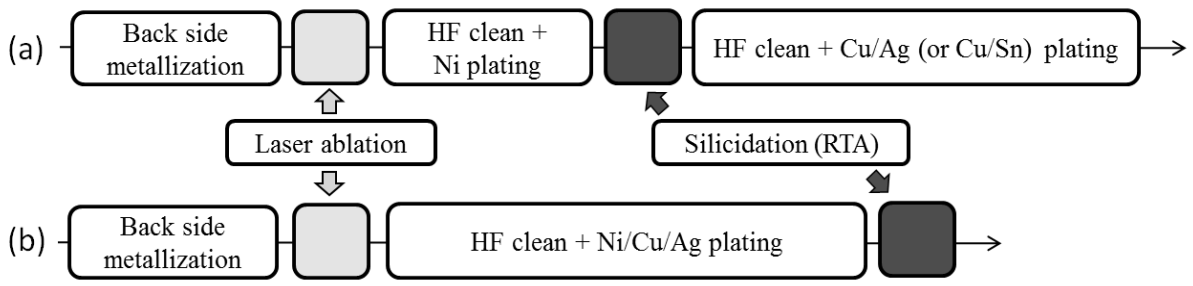


Figure 5.26: Schematic of a self-aligned plating sequence where nickel silicidation (Rapid Thermal Annealing) is performed (a) directly after Ni plating or (b) after completion of the full Ni/Cu/Ag metal stack.

The development of a simplified plating sequence where sintering is performed after Ni/Cu/Ag plating requires to: (i) control nickel silicide formation of thick Ni layers, (ii) ensures sufficient mechanical adhesion, and (iii) demonstrates long-term reliability. Control of nickel silicide formation is discussed here while the latter two points are discussed in Chapter 7.

For thin PVD Ni seed layers, it was shown in section 5.2.2 that low temperature silicidation enables improved control of Ni_2Si formation (diffusion-limited) and leads to reduced junction damage. It was also shown that the Ni_2Si phase is sufficient to contact lowly doped emitters down to surface concentrations around $1x10^{19}$ cm^{-3}. Therefore, the strategy adopted was to adapt the thermal budget for the silicidation of a thick (~1 µm) LIP Ni layer to match the Ni_2Si thickness obtained after silicidation of a thin (40 nm) PVD Ni layer. In a second stage, the sintering step is moved to after Cu/Ag plating and the impact on junction damage is compared to sintering prior to Cu/Ag plating. Specific contact resistance and pull tab adhesion measurements are also performed to demonstrate that sintering at the end yields the required properties.

Large area (12.5x12.5 cm^2) p-type magnetically pulled CZ-Si wafers (m-CZ-Si) were processed into i-PERC solar cells according to the sequence given in Figure 5.27.

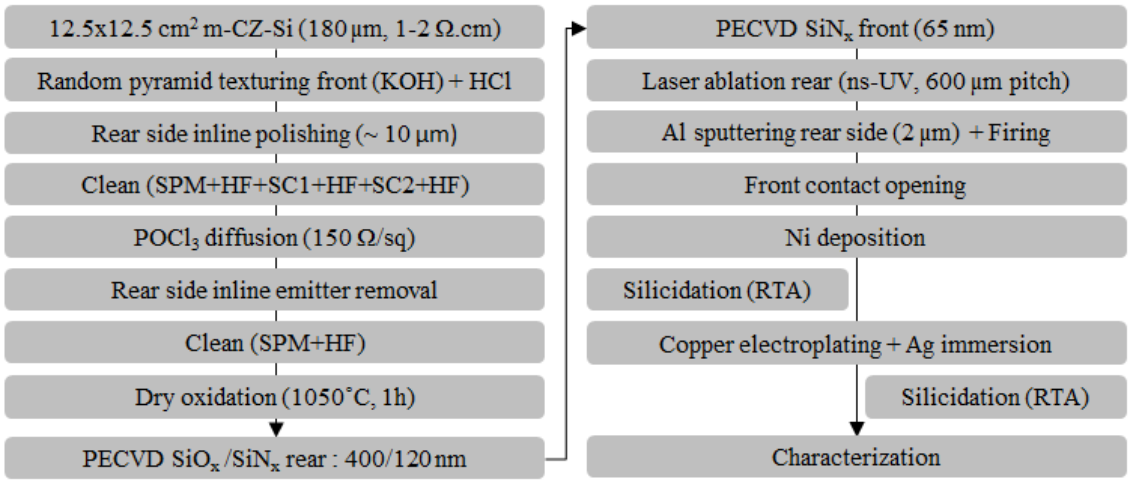


Figure 5.27: Process sequence diagram for p-type i-PERC solar cells on magnetically pulled CZ-Si wafers (m-CZ-Si) featuring an homogeneous 1 µm deep 120 Ω/sq and nickel/copper plated front contacts.

As compared to previous tests performed with PVD Ni or electroless Ni seed layer, thermal oxidation was performed at 1050˚C resulting in 1 μm deep 120 Ω/sq homogeneous emitter with a low surface concentration ~1x10^{19} cm^{-3}. Emitter optimization is further discussed in Chapter 6. To eliminate any potential wafer contamination issue prior to $POCl_3$ diffusion, an extensive wafer cleaning sequence described as "full-RCA" was also implemented. This cleaning sequence consists of SPM (H_2O_2:H_2SO_4: 1/5, 90˚C, 10 min), SC1 (NH_4OH:H_2O_2:H_2O: 1/1/4, 60˚C, 10 min), SC2 (HCL:H_2O_2:H_2O: 1/1/4, 60˚C, 10 min) with intermediate rinsing steps in de-ionized water and intermediate HF dips (HF:HCL:H_2O: 2/2/96, 2 min).

At first, front contact openings were defined by photolithography to form several mini-cells (area=5x5 cm^2) per wafer. After removal of the photo-resist and opening the front $SiN_{x\ in}$ buffered HF, nickel was deposited either by sputtering (Ni=40 nm) or by light-induced plating (Ni~1 μm). Mini-cells were laser diced and silicidation was performed under N_2 at 300˚C for various durations. Unreacted Ni was removed in HNO_3 (20% HNO_3, T=25˚C, 10 min) and sheet resistance (R_{sh}) measurements (4 point probe) were performed in the busbar areas of the mini-cells. Since nickel silicide formation is diffusion-limited, R_{sh} (proportional to 1/thickness) results are plotted versus square root of time as shown in Figure 5.28a. From these results, equivalent R_{sh} as with sintering 40 nm PVD Ni for 30s can be obtained with 1 μm of LIP Ni by increasing the sintering time to about 120 seconds. In case of sintering after completion of the full Ni/Cu/Ag stack (Ni/Cu/Ag: 1/9/0.1 μm), the required sintering time is slightly longer.

Similarly, the pseudo Fill-Factor (pFF) of these mini-cells was evaluated for various sintering durations at 300˚C and results are given in Figure 5.28b. All pFF values obtained, be it for sintering before or after completion of the full Ni/Cu/Ag stack, are above 82% even for sintering durations up to 10 min. This demonstrates that, in case of wet etch patterning of a 1 μm deep emitter, moving the sintering step after Ni/Cu/Ag plating does not lead to significant junction damage.

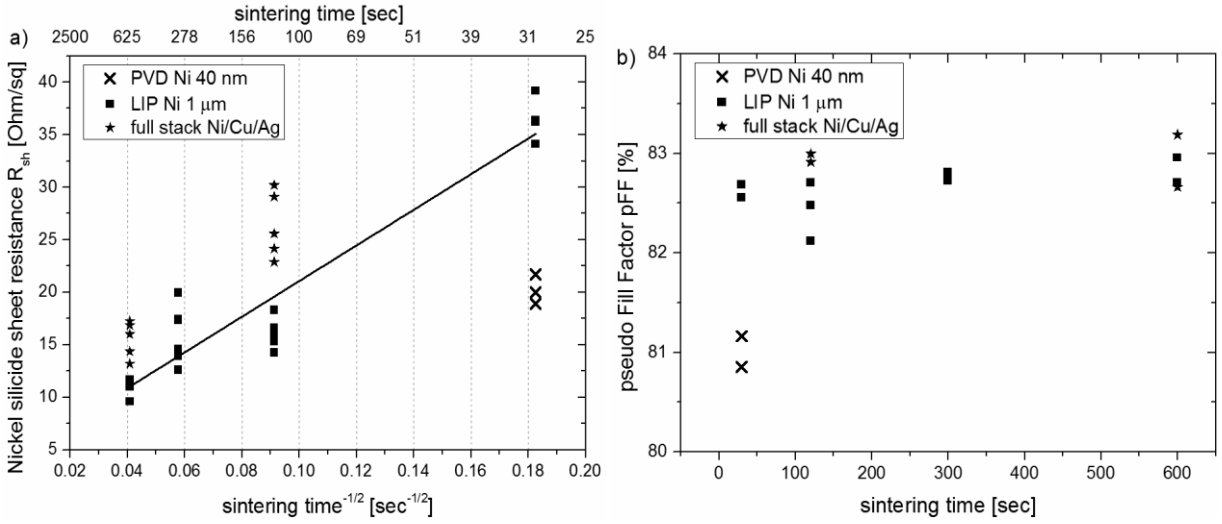


Figure 5.28: a) Sheet resistance measured after unreacted nickel removal for various sintering durations at 300˚C. b) Pseudo Fill Factor measured for various sintering durations at 300˚C on wet-etched opened dielectrics.

However, pFF values were found to drop well below 80% for 10 min sintering in the case of ps-UV laser ablated SiN_x (the optimization of ps-UV laser ablation is discussed in Chapter 6). Therefore, the sintering temperature was dropped to 250 ˚C to better control Ni_2Si formation and ramping/cooling rates were lowered to 50˚C/min (instead of 600 ˚C/min) as this helps substituting RTA for belt furnace annealing in the future. From the results given in Table 5.4, pFF values above 82% can be maintained for durations up to 10 min. Interestingly, the process window is extremely large since the fill factor only improves marginally after 30s annealing. Also interesting to observe, is the fact that sintering lowers the busbar-to-busbar resistance (i.e. finger resistance) by about 10% but also increases open-circuit voltage, short-circuit current density, and fill factor.

Improvements in the electrical parameters upon sintering were confirmed on full area (12.5x12.5 cm^2) ps-UV laser ablated cells where average efficiencies around 20% were obtained by performing a 250˚C, 4 min sintering after completion of the Ni/Cu/Ag stack. As shown in Table 5.5, these results are equivalent to the best results obtained in a separate experiment with a thin 40 nm PVD Ni seed layer and sintering for 4 min at 300˚C prior to subsequent Ni/Cu/Ag plating. Improvements in open-circuit voltage and short-circuit density upon sintering are discussed in Chapter 6 together with process optimization. Improvements in finger resistance and fill factor upon sintering are discussed below.

Table 5.4: Electrical parameters for i-PERC solar cell measured after completion of the full Ni/Cu/Ag front metal stack for various sintering durations at 250˚C, ps-UV laser ablation was used to define the front contact openings.

Sintering duration at 250˚C	FF [%]	n	pFF [%]	R_{bb} [mΩ]
before sinter	77.3	1.08	81.9	36.6
0.5 min	78	1.08	82.1	31.5
1 min	78	1.08	82.1	31.3
4 min	78	1.08	82.1	31.2
10 min	78.1	1.09	82.0	31.2

Table 5.5: Average (over 4 cells) electrical parameters for large area (12.5x12.5 cm^2) i-PERC solar cells measured after completion of the full Ni/Cu/Ag front metal stack and after sintering at 250˚C for 4 min under N_2. Solar cells with 40 nm PVD Ni seed layer were processed separately and sintering was performed at 300˚C for 4 min under N_2 directly after Ni deposition, unreacted Ni was removed in 20% HNO_3, and the surface was re-activated in 1%HF prior to Ni/Cu/Ag plating. For all groups, ps-UV laser ablation was used to define the front contact openings.

Front metallization	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	ŋ [%]	J_{02} [A/cm^2]	r_s [Ω.cm^2]	n	pFF [%]	R_{bb} [mΩ]
Ni/Cu/Ag before sintering	38.4	648.4	77.9	19.4	$3x10^{-08}$	0.81	1.1	82.3	37.9
Ni/Cu/Ag after sintering	38.6	655.5	78.9	20.0	$2x10^{-08}$	0.63	1.1	82.2	33.8
PVD Ni + etch +Ni/Cu/Ag	38.5	656.3	79.0	20.0	$2x10^{-08}$	0.53	1.2	81.8	36.7

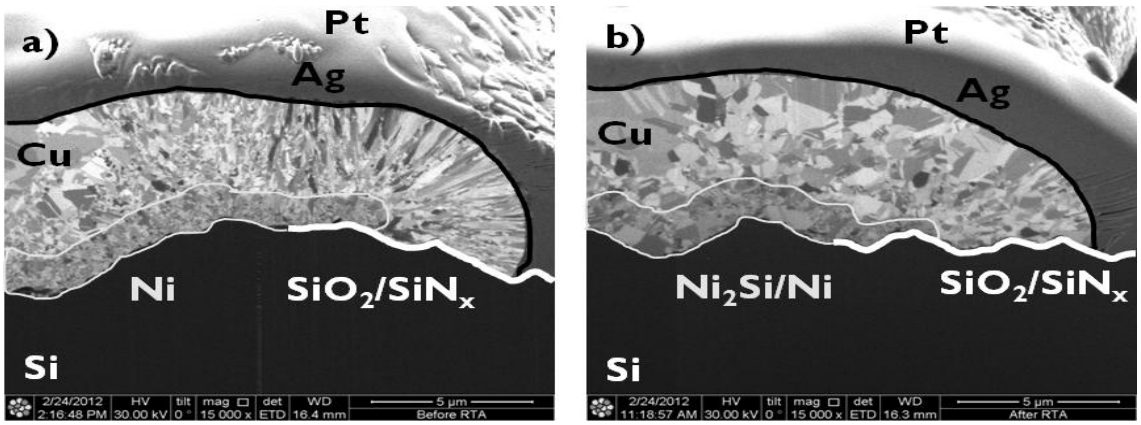


Figure 5.29: Focused ion beam (FIB) images (a) before and (b) after sintering Ni/.Cu/Ag for 4 min at 250˚C. Pt is added as a contrast layer during sample preparation.

Cross-section focused ion beam (FIB) images were taken, prior to and after sintering, of Ni/Cu/Ag plated fingers to reveal any change in microstructure that would explain the measured 10% drop in finger resistance upon sintering. FIB images are shown in Figure 5.29. Upon sintering, the columnar radially oriented Cu grains have reorganized into larger Cu grains. Nickel grains are also found to re-organize upon sintering. Ni is more resistive than Cu and the Ni plated thickness (~1 µm) is much less. Therefore, the drop in finger resistance can be mostly attributed to the change in Cu microstructure leading to lower electron grain boundary scattering as described by the Mayadas-Shatzkes model [MAY70]. Re-organization of plated Cu into larger grains has also been reported in literature at room temperature and has been described as self-annealing. Investigations performed by Stangl and coworkers [STA05] revealed that the change in resistivity during self-annealing can be divided into two periods. During the first period, organic impurities incorporated mainly in free volumes between grains diffuse towards the surface leading to an almost stress-free stage by stress relaxation. The reached stress-free stage marks the beginning of the second period of accelerated grain growth. Thus, it is very likely that sintering only accelerates the kinetics of self-annealing and that plating chemistries strongly affect the measured change in finger resistance. Experiments were performed using a low-stress Cu chemistry (Enlight470 from DOW instead of a Cu GLEAM chemistry from DOW) and no change in finger resistance could be measured upon sintering. Plating chemistries and changes in microstructure upon sintering might also play an important role in the final adhesion of the Ni/Cu/Ag plated contacts and hence further investigations are planned in this direction.

Despite the fact that Ag is much more expensive than tin (Sn), immersion Ag plating is seen as cost competitive since, as also shown in these FIB images, a thin (~100-200 nm) and continuous Ag layer can be obtained whereas this is quite challenging to achieve with Sn since it is typically electroplated. Finally, FIB images also revealed the presence of voids at the interface between Cu and the SiO_2/SiN_x passivation. Such voids can be understood by the poor adhesion of Cu onto dielectrics and the intrinsic stress of the deposits. This has significant implications since SiO_2/SiN_x might not be the weakest point to Cu diffusion and since adhesion to Si has to be provided by the thin Ni layer which accounts for only a third to a half of the total finger area.

Apart from the measured reduction in finger resistance, a reduction in specific contact resistance can also contribute to the observed reduction in series resistance upon sintering. Specific contact resistance (ρ_c) measurements were performed using TLM (see appendix A) test structures that were laser diced from solar cells after Ni/Cu/Ag plating. Using such test structures presents the advantage that ρ_c can be measured prior to and after sintering. The results, given in Figure 5.30a, indicate that excellent ρ_c values in the range of 0.2 to 1 mΩ.cm^2 can be obtained already after Ni/Cu/Ag even though the surface concentration is relatively low (N_s~1x10^{19} cm^{-3}). Upon sintering the full Ni/Cu/Ag stack at 250˚C, measured ρ_c values reduce do below 0.1 mΩ.cm^2 and the reduction is attributed to Ni_2Si formation. Such low ρ_c values are well within the target value of 0.5 mΩ.cm^2 that was defined in Chapter 4. Interestingly, higher sintering temperatures do not appear to further improve ρ_c values. Though it is difficult to compare our data with literature, it is worth mentioning that sintering temperatures around 350˚C were found optimum (ρ_c~0.5 mΩ.cm^2) for LDSE (Ns> 1x10^{20} cm^{-3}) solar cells plated using non-contact LIP Ni [TJA10]. In the case of electroless Ni seed layers, ρ_c values were found to steadily decrease with sintering temperature down to 0.1 and 0.01 mΩ.cm^2 after sintering at 500˚C for lowly doped (N_s~1x10^{19} cm^{-3}) and highly doped ($N_{s>}$1x10^{20} cm^{-3}) emitters respectively [BRA10]. Our results confirm that formation of nickel silicide can be achieved even at sintering temperatures as low as 250˚C which is interesting to minimize both Ni and Cu diffusion and hence junction damage. This is a key aspect in this simplified process sequence and hence particular care was taken during the thesis in making sure that $\rho_c \leq$0.1 mΩ.cm^2 could be achieved after sintering at 250 ˚C.

Pull tab adhesion (for further details see Chapter 7) measurements were also performed to evaluate mechanical adhesion to Si. The results, shown in Figure 5.30b, confirm that the simplified process sequence consisting of: (i) laser ablation, (ii) HF/Ni/Cu/Ag plating sequence, and (iii) sintering at 250˚C for 4 min, leads to comparable adhesion results as with more elaborated process sequence where sintering is performed prior to Cu plating.

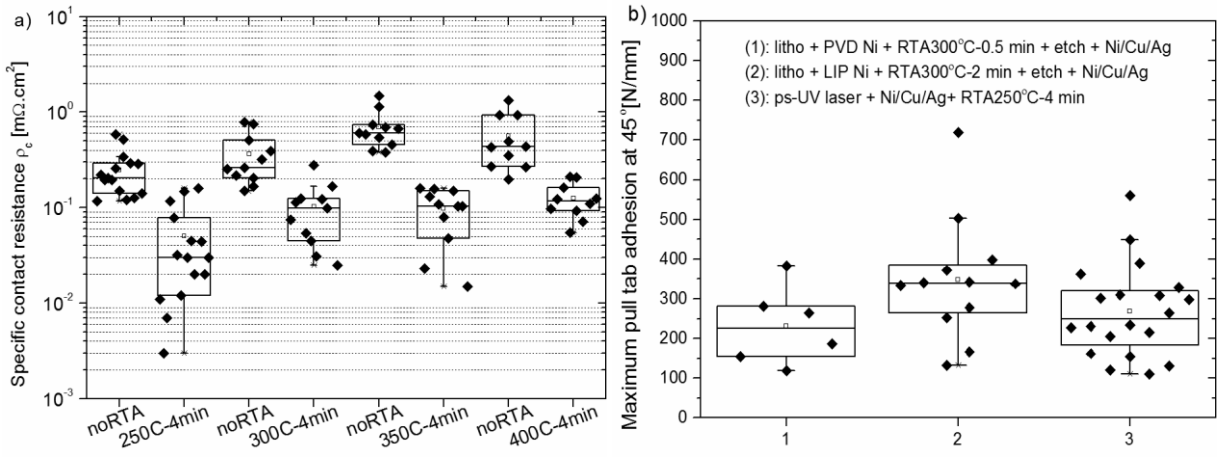


Figure 5.30: a) Specific contact resistance vs. rapid thermal annealing temperature (performed after Ni/Cu/Ag plating) for i-PERC solar cells featuring a lowly doped 120 Ω/sq emitter (N_s~1x10^{19} cm-3). b) Maximum pull tab adhesion data measured at 45˚ for various front side metallization sequence.

5.4.4. Transfer to pilot production sintering tool

As a step towards demonstrating industry viability of this simplified plating sequence, two commercially available pilot production sintering tools with a throughput over 100 wafers/hour were evaluated. In both systems, wafers are transported onto a conveyor belt across a heated section filled with nitrogen to minimize oxygen levels. The BTU VMCA system uses a muffle heated section with fully enclosed coil heaters located at the top and bottom of the process chamber. The SL sintering furnace from Despatch uses a clam shell design and consists in 10 infra-red (IR) heated zones. The BTU VMCA is specified for oxygen levels below 5 ppm while the Despatch system can maintain levels below 100 ppm.

Large area (12.5x12.5 cm^2) wafers were processed into i-PERC solar cells according to the sequence given in Figure 5.27. The front metallization was defined using the developed simplified plating process (ps-laser + HF/Ni/Cu/Ag + sintering). Illuminated I-V results measured prior to and after sintering of the best solar cells are given in Table 5.6. For both sintering systems, efficiencies close to 20% were obtained which are comparable with previous results obtained by RTA at imec. As observed before, fill factor, open-circuit voltage, and short-circuit current densities values improved upon sintering while R_{bb} values dropped. For the samples sintered at Despatch ($[O_2]$~100 ppm), it is interesting to observe that, despite the Ag capping, some degree of discoloration due to Cu oxidation could be observed after sintering. However, apart from affecting aesthetics, this did not appear to affect electrical results. Finally, the decision was made to purchase the BTU VMCA sintering tool and the system is operational at imec since early 2013.

Table 5.6: Best illuminated I-V parameters for large area (12.5x12.5 cm^2) i-PERC solar cells using a simplified plating sequence. Solar cells were measured after completion of the full Ni/Cu/Ag front metal stack and after sintering at 250˚C for 4 min under N_2. Sintering was performed externally at BTU or at Despatch.

Sintering tool	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	ŋ [%]	r_s [$\Omega.cm^2$]	n	pFF [%]	R_{bb} [mΩ]
BTU before sintering	37.9	654	78.9	19.6	0.57	1.16	81.9	41.6
BTU after sintering	38.1	659	79.3	19.9	0.48	1.18	81.8	39.9
Despatch before sintering	38.2	656	77.9	19.5	0.768	1.17	81.8	39.9
Despatch after sintering	38.4	659	78.5	19.8	0.61	1.2	81.5	38.3

5.4.5. Transfer to pilot production plating tool

As an another step towards demonstrating industry viability of this simplified plating sequence, pilot production plating tools from different equipment manufacturers (RENA, Gebr. SCHMID, and MECO) were evaluated during the course of this thesis. A decision was made by imec to purchase a pilot production plating from Meco and this system is operational at imec since mid-2012. The MECO DPL plating tool present at imec was designed in collaboration with MECO so that it would be compatible with the simplified plating sequence developed in this thesis and offer a high degree of flexibility.

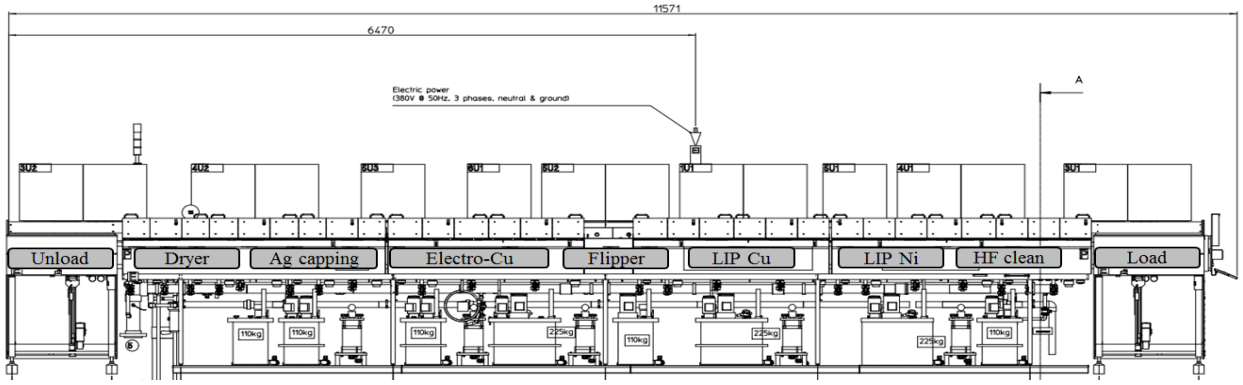


Figure 5.31: Schematic of the MECO DPL plating tool installed at imec enabling HF/Ni/Cu/Ag in one sequence. Wafers are transported vertically from right to left across the different plating modules labeled in grey.

In the MECO DPL plating system installed as imec, wafers are automatically loaded (and unloaded) by a robot to a stainless steel belt which transports the wafers at a constant speed vertically across successive modules, as shown in Figure 5.31. The HF cleaning and plating modules feature a lower heated storage tank and an upper tank for processing. During processing, constant liquid level and agitation are achieved in the upper tank by pumping enough solution to balance liquid flowing over the rim of the tank as shown in Figure 5.32a. Liquid flowing over the rim is then filtered and re-circulated. The vertical design minimizes solution drag-out (see paragraph below), enables a constant electrical contact to the wafers, and ensures that each wafer "sees" the same plating conditions (distance to anode, etc.). Metal "hold" clips, as shown in Figure 5.32b, hold the wafer in position against back contact clips which are electrically connected to the metal belt. Back contact clips are used to apply a bias to the rear side of the wafers during bias-assisted LIP. Dedicated clips are also present at the front side. These front contact clips come in contact with the front busbars to enable electroplating after the wafers pass through a simple mechanical contact flipper. During contact flipping, the rear contact clips are retracted so that current applied to the metal belt is distributed, via the front contact clips, only to the front side of each wafer present in the bath. Despite the important number of contacts, acceptance tests performed at imec on thin wafers (thickness~140 μm) revealed no issues with breakage rate (well below 0.1%) nor with within wafer and wafer-to-wafer plating uniformity.

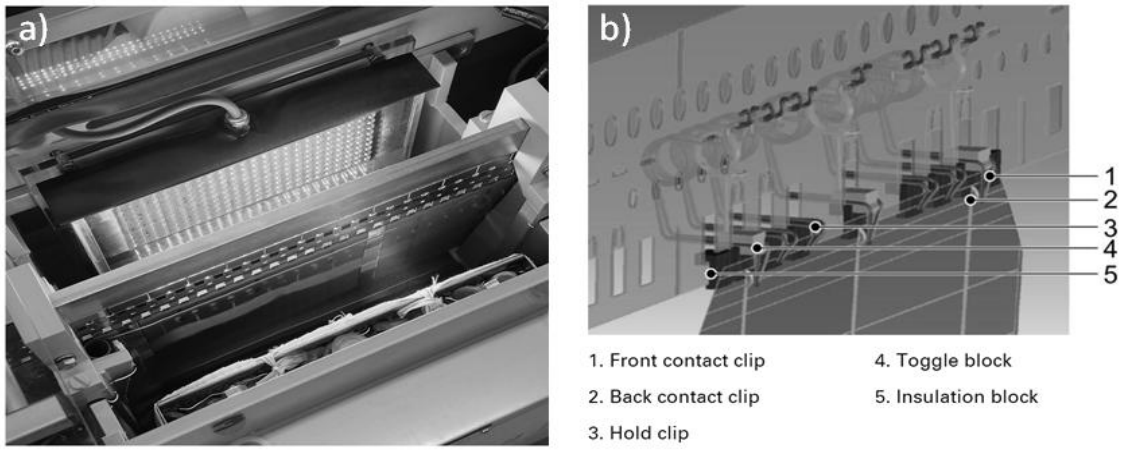


Figure 5.32: a) Picture of a bias-assisted LIP Ni processing tank in the MECO DPL plating tool. b) Computer drawing of a three busbars wafer attached to a metal belt showing the various clips and their respective functions. Images with the courtesy of MECO.

The length of each modules was designed to obtain a throughout over 100 wafers/hour for a plating sequence consisting of: (i) HF clean, (ii) bias-assisted LIP Ni, (iii) bias-assisted LIP Cu, (iv) electroplating of Cu, (v) Ag capping, and (vi) drying. The presence of a bias-assisted LIP Cu step in this sequence increases the seed layer conductivity which improves thickness uniformity of the electroplating Cu step. It also enables the use of thinner LIP Ni seed layers if desired or to plate solar cells without front busbars (not possible with electroplating). Between each modules, wafers are rinsed in de-ionized water using spray-rinses to minimize water consumption and hence costs associated with treatment of metal-contaminated rinse water. After water rinsing, wafers pass through air-knives which minimize water transport into the plating baths (i.e. drag-in) thus preventing dilution of the electrolytes. In that respect, non-only vertical transport minimizes drag-in but it also reduces electrolyte drag-out.

The MECO DPL plating tool offers some degree of flexibility since one or several plating steps can be skipped by keeping the electrolyte in the lower storage tank. The length of the LIP Ni and LIP Cu processing tanks can also be adjusted to some extent. Finally, the Ag capping can be deposited either by electroplating, bias-assisted LIP, or immersion.

Compared to the single wafer bias-assisted LIP and electroplating setups used in the lab, the inline MECO DPL plating tool presents some advantages but also some disadvantages. Apart from the clear advantage of throughput, the MECO DPL plating tool presents the advantage that wafers move in front of the anodes instead of being static. This greatly helps improving within wafer and wafer-to-wafer thickness uniformity especially for bias-assisted LIP since the distance to the LED light-source is better maintained in the MECO DPL tool. However, an inline tool presents the disadvantages that testing new plating solutions is costly (large volumes) and that the timing of each step cannot be independently controlled.

Timing is a key notion to understand in an inline tool as the length of each section and the constant belt speed define the time in the HF cleaning section, the time in the rinse-section after HF, the time entering the bias-assisted LIP Ni section, the time in the bias-assisted LIP Ni, and

so forth. Timing can have a dramatic impact on contact resistance but also on mechanical adhesion. For the MECO DPL tool, timing issues were considered early-on (tool design phase) but also required minor hardware changes once the tool was installed at imec. Results presented below were obtained in one plating sequence (load, HF/Ni/Cu/Ag, unload) at a constant speed once these hardware changes were implemented.

As presented next in Chapter 6, a power-loss analysis was conducted on the best 12.5x12.5cm^2 p-type i-PERC device (20.5% efficiency) obtained with the process sequence described in Figure 5.27. This power-loss analysis led to the optimization of several process steps on 15.6x15.6cm^2 substrates when using the MECO DPL plating tool and the BTU VMCA sintering tool. Following this optimization, average efficiencies of 20.5%, with a low standard deviation of 0.1%, were obtained on 109 wafers. The best solar cell resulted in an energy conversion efficiency of 20.7% as shown in Table 5.7 which is the highest efficiency measured during the course of this PhD thesis.

Table 5.7: Average and best illuminated I-V parameters for large area (15.6x15.6 cm^2) i-PERC solar cells featuring a 120 Ω/sq 0.6 μm deep emitter (see Chapter 6). The front contacts were plated in one sequence (HF/Ni/Cu/Ag) in the MECO DPL plating tool and sintered for 4min at 250˚C in the BTU VMCA sintering tool.

Device	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	ŋ [%]
Average (109 wafers)	38.8	661.3	80.0	20.5
Standard deviation	0.1	1.2	0.2	0.1
Best solar cell	39.1	661.7	80.0	20.7*

*Externally confirmed at FhG ISE CalLab

To the best knowledge of the author, only Schott Solar is currently (i.e. August 2013) reporting higher solar cell efficiencies on large area p-type CZ-Si solar cells (21.3%, Metz et al. [MET13]). Comparing specific contact resistance measurements and pull tab adhesion measurements performed on these cells with previous cells plated and sintered using single wafer laboratory setups, equivalent results (average ρ_c~0.1 mΩ.cm^2, average pull adhesion values at 45˚>2 N/mm) could be demonstrated using the pilot production MECO DPL plating and BTU VMCA sintering systems. Therefore, we can conclude that the simplified Ni/Cu/Ag plating sequence developed in this thesis was successfully transferred to pilot production plating and sintering tools installed at imec.

5.5. Discussion of results

In this chapter, various metal layers were investigated as possible "seed" layers prior to Cu electroplating. Ideally, a seed layer should provide low specific contact resistance to lowly doped silicon, sufficient mechanical adhesion, and act as a barrier against Cu diffusion. In addition, the seed layer deposition method and the processing sequence should be simple, fast, cost-effective, and enable the formation of narrow metal fingers (<30 μm wide).

In the first part of this chapter, ns-UV laser ablation of the front SiN_x anti-reflective coating was evaluated as an alternative to photolithography (wet etch) patterning. Front contacts were defined using sputtered (PVD) Ti/Cu seed layers and a photolithography lift-off sequence prior to Cu electroplating. Process conditions to minimize junction damage using ns-UV laser ablation were described and equivalent solar cells results could be demonstrated. Solar cells were then processed with various PVD seed layers (such as Ta or TaN), known from the semiconductor industry as good barriers to Cu diffusion, and compared with solar cells featuring PVD Ti or Ni seed layers. Solar cells with a PVD Ni seed layer were shown to lead to comparable results as solar cells processed with other seed layers.

In the second part of this chapter, self-aligned silicide (SALICIDE) contacts using PVD Ni were investigated. It was shown that nickel-silicide formation is diffusion-limited and that low temperature silicidation (leading to Ni_2Si phase) was preferred to minimize junction damage. From the different analysis performed, it is speculated that even though nickel silicide thickness can be controlled to stay below 50 nm, defects generated during ns-UV laser ablation on alkaline textured surfaces can lead to pseudo fill-factor degradation on 450 nm deep junctions. Using 600 nm deep junctions, efficiencies up to 19.4%, equivalent to cells with PVD Ti/Cu lift-off, were demonstrated using a photolithography-free ("litho-free') sequence. This "litho-free" sequence consists of: (i) laser ablation, (ii) thin 40 nm PVD Ni deposition, (iii) rapid thermal annealing, (iv) unreacted Ni etch, (v) HF clean, and (vi) subsequent Ni/Cu/Ag plating steps.

In the third and fourth parts of this chapter, electroless and bias-assisted light-induced plating (LIP) of nickel were evaluated as an alternative to PVD Ni. Mechanisms were proposed to explain the measured presence of oxygen at the interface with Si when using an alkaline electroless NiP solution. Nickel Silicidation kinetics were shown to be slower for alkaline electroless NiP deposits than with PVD Ni, possibly due to the presence of oxygen and phosphorous. In the case of bias-assisted LIP Ni, deposition on silicon was described and silicidation at temperature as low as 250˚C (similar to PVD Ni) could be demonstrated. The properties of alkaline electroless NiP and bias-assisted LIP Ni deposits obtained in this chapter as compared to PVD Ni or PVD Ti/Cu seed layers are summarized in Table 5.8.

In the last part of this chapter, using bias-assisted LIP Ni deposition, a simplified "litho-free" plating sequence was described which consists of: (i) laser ablation, (ii) a HF/Ni/Cu/Ag sequence, and (iii) sintering at 250˚C for 4 min. In this sequence all metal layers are deposited by plating and, as shown in Table 5.9, the number of individual steps required for the front side metallization is down to 6 steps as compared to 14 steps for a SALICIDE sequence. In addition,

this simplified plating sequence was successfully transferred to pilot production plating and sintering tools. Using these tools and implementing process improvements which are discussed next in Chapter 6, average efficiencies of 20.5% (over 109 wafers) and top efficiency of 20.7% were demonstrated on industrial size (15.6x15.6 cm^2) p-type PERC solar cells. Therefore, next steps towards demonstrating industrial viability for this simplified plating sequence include demonstrating: (i) long-term reliability (Chapter 7), and (ii) reduced cost-of-ownership as compared to solar cells with screen printed Ag front contacts (Chapter 10).

Table 5.8: Summary table with the different properties of the various seed layers evaluated in this chapter. Mechanical adhesion and diffusion barrier properties are further discussed in Chapter 7.

	PVD Ti/Cu (or alternative to Ti)	PVD Ni	Electroless NiP (pH=10)	Bias-assisted LIP Ni
Deposition rate	- (>30 nm/min)	- (>30 nm/min)	+ (>80 nm/min)	+++ (>400 nm/min)
Thickness uniformity	+++ (± few nm)	+++ (± few nm)	++ (± 20 nm)	+ (only >200 nm)
Mechanical adhesion	+++	+ (need surface activation after unreacted Ni etch)	+ (only for NiP <350 nm)	++
Diffusion barrier to Cu	+++ (CMOS barrier)	- (thin Ni_2Si sufficient?)	+ (NiP better than pure Ni?)	++ (thick Ni possible)
Process	++ (no sintering) - (not self-aligned) - (high vacuum) - (material waste)	+ (self-aligned Ni_xSi) - (high vacuum) - (material waste)	++ (self-aligned NiP) ++ (no high vacuum) - (bath lifetime)	++ (self-aligned Ni) ++ (no high vacuum) ++ (stable bath)

Table 5.9: Process simplification for the front side metallization of p-type PERC cells demonstrated in this chapter.

"Lift-off" sequence (10 steps)	SALICIDE sequence (14 steps)	"Litho-free" (9 steps)	Simplified "litho-free" (6 steps)
Spin resist	Spin resist		
Bake resist	Bake resist		
UV illumination	UV illumination		
Bake resist	Bake resist		
Develop resist	Develop resist		
BHF SiN_x opening	BHF SiN_x opening	Laser ablation SiN_x	Laser ablation SiN_x
	Resist removal	HF clean	HF clean
PVD Ti/Cu: 30/150 nm	PVD Ni 40 nm	Ni seed layer (PVD, Electroless, or LIP)	LIP Ni (~1 μm)
Lift-off	Sinter (RTA)	Sinter (RTA)	
	Unreacted Ni etch	Unreacted Ni etch	
	HF clean	HF clean	
	LIP Ni (~1 μm)	LIP Ni (~1 μm)	
Electro-Cu	Electro-Cu	Electro-Cu	Electro-Cu
Ag immersion	Ag immersion	Ag immersion	Ag immersion
			Sinter (RTA)

CHAPTER 6

Optimization of p-PERC Si solar cells with fully plated contacts sintered at the end

This chapter describes the optimization of several processes that were performed when transferring the simplified Ni/Cu/Ag plating sequence (see previous chapter) to industrial size 15.6x15.6 cm^2 substrates. A simple analytical power-loss analysis of the best 12.5x12.5 cm^2 p-type i-PERC device (η=20.5%) is presented in the first part of this chapter as it was the basis on which the process optimization was conducted. Areas of improvements enabling efficiencies beyond 21% were identified using PC1D simulations and some of these areas were investigated in this thesis. Namely, these include: front homogeneous emitter profile (section 6.2.1), bulk CZ-Si material (section 6.2.2), front dielectric(s) (section 6.2.3), front ps-UV laser ablation (section 6.2.4), front metal grid (section 6.2.5), and internal rear reflectance (section 6.2.6).

6.1. Power loss analysis

Fast analytical power-loss methods have been proposed for conventional H-pattern [ABE11] and for high-efficiency interdigitated back contact (IBC) silicon solar cells [VER12c]. Such models provide a detailed quantification of the different loss mechanisms in mW/cm^2 which helps directing future process improvements based on the most important contributions. Following those proposed methods, a power-loss analysis was performed on the best p-type i-PERC solar cell obtained on 12.5x12.5 cm^2 magnetically pulled CZ-Si (m-CZ-Si) using the simplified plating sequence developed in Chapter 5. This sequence is shown again in Figure 6.1. Potential improvements in cell efficiencies were then estimated and their process implementation is discussed in the rest of this chapter.

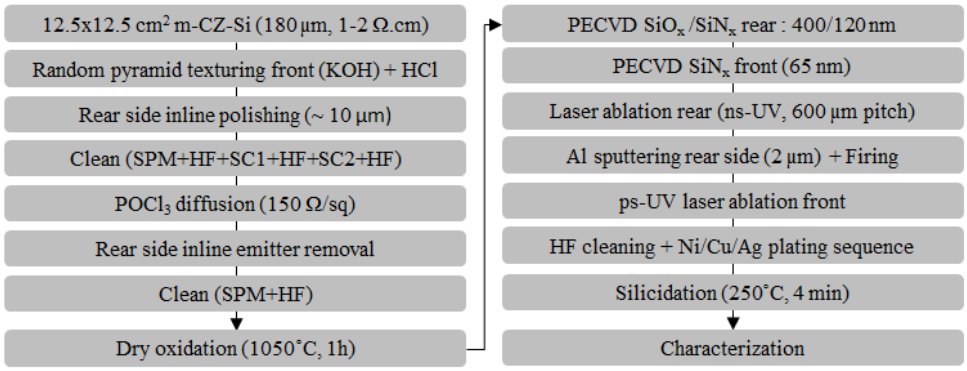


Figure 6.1: Process sequence for p-type i-PERC cells on magnetically pulled CZ-Si wafers (m-CZ-Si) featuring an homogeneous 1 µm deep 120 Ω/sq and Ni/Cu/Ag front contacts plated in one sequence and sintered at the end.

The measured light I-V parameters of the best 12.5x12.5 cm^2 i-PERC cell obtained in this thesis are presented in Table 6.1. For comparison, the best I-V results obtained by Schott Solar [MET13] together with theoretical maximum values are also given in Table 6.1. To the best knowledge of the author, the Schott Solar I-V data represents the best published results to date (i.e. August 2013) on large area (15.6x15.6 cm^2) p-type solar cells.

Table 6.1. Best cell illuminated I-V results for p-type PERC solar cells with Ni/Cu front contacts compared with theoretical maximum values. Power losses due to non-maximum value for the best cell are also given as indication.

parameter	V_{oc} (mV)	j_{sc} (mA/cm^2)	FF (%)	eta (%)
This thesis, best 12.5x12.5 cm^2 cell	665.2	38.6	79.9	20.5*
Schott Solar, best 15.6x15.6 cm^2 cell [MET13]	665	39.9	80.5	21.3*
Estimated maximum values**	756.3	44.0	89.3	29.7
Power loss of best 12.5x12.5 cm^2 cell in this thesis due to non-maximum value [mW/cm^2]	3.35	3.75	2.14	9.24

*Calibrated measurement at the Fraunhofer ISE, with AM1.5g IEC60904-3Ed.2 (2008)

**Calculated with n_i=9.65x10^9 cm^{-3} at 300K [WOL10] and not n_i=1.0x10^{10} cm^{-3} as in [VER12c] which gives a higher maximum Voc and consequently a maximum eta above 29.6%.

The maximum short circuit current density j_{max} is calculated through the integration of the AM1.5g solar spectrum assuming the Lambertian limit for the rear reflectance and a wafer thickness W=160 µm. The maximum open-circuit voltage ($V_{oc,max}$) is obtained assuming Auger recombination is the only recombination mechanism with C_A=1.66x10^{-30} cm^6/s and using n_i=9.65x10^{-9} cm^{-3} (at T=300 K) for the intrinsic carrier density [WOL10]. In a first approximation, the maximum fill factor is obtained from an empirical expression [GRE81] as:

$$FF_0 = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \quad (6.1)$$

$$\text{with } v_{oc} = \frac{qV_{oc,max}}{nkT} \quad (6.2)$$

where *q* is the electron charge, *n* the ideality factor (n=2/3 when limited by Auger recombination), *k* the Boltzmann constant, and *T* the absolute temperature.

The individual power loss of the best cell due to non-maximum values, presented in table 6.1, are calculated as follows. The maximum FF with the real V_{oc} (FF_{0V}) is obtained from equation (6.1) using the measured V_{oc} (i.e. 665.2 mV) in equation (6.2) leading to a power loss due to non-maximum FF (FF_{PLoss}):

$$FF_{PLoss} = FF_{0V} * j_{sc,meas.} * V_{oc,meas.} - FF_{meas.} * j_{sc,meas.} * V_{oc,meas.} \quad (6.3)$$

The power loss due to non-maximum V_{oc} ($V_{oc,PLoss}$) is obtained according to:

$$V_{oc,PLoss} = FF_{0I} * j_{sc,meas.} * V_{oc,calc.} - FF_{0V} * j_{sc,meas.} * V_{oc,meas.} \quad (6.4)$$

$$\text{with } V_{oc,calc.} = \frac{2kT}{3q} \ln\left(\frac{j_{sc,meas.}}{qC_A W n_i^3}\right) \quad (6.5)$$

and with FF_{0I} obtained from equation (6.1) using $V_{oc,calc.}$ in equation (6.2). Finally, the power loss due to non-maximum j_{sc} is obtained by subtracting FF_{PLoss} and $V_{oc,PLoss}$ from the maximum theoretical power (29.7 mW/cm^2).

As can be seen from Table 6.1, the 20.5% cell is strongly limited by a 1.3 mA/cm^2 absolute difference in j_{sc} compared to the record cell reported by Schott Solar. The total reflectance (including busbars), external quantum efficiencies (EQE), and internal quantum efficiencies (IQE) are presented in Figure 6.2a. Using the measured EQE values, the integrated current density is 38.6 mA/cm^2 which is in good agreement with the measured j_{sc} given in Table 6.1. The light trapping parameters: backside reflectance R_b, number of light passes Z_0, and optical absorption thickness Z_0*W were calculated, following the method proposed by Rand and Basore [RAN91], from the linear fit of 1/IQE versus the absorption depth (1/α) as shown in Figure 6.2b. They were estimated at 95.1%, 25.4, and 4.1 mm respectively. By performing additional measurements, the reflectance, IQE, and EQE of the active area (area in between the fingers) can be determined (not shown here). The front surface escape loss (i.e. light that entered the solar cell, was not absorbed, and escaped through the front surface) is calculated by integrating the active area primary reflectance over the AM1.5g spectrum in the range of 1000-1200 nm [ABE11]. The front surface reflectance loss is calculated by integrating the active area primary reflectance over the AM1.5g spectrum in the range of 300-1200 nm. Finally, the front grid shading loss is obtained from the difference between the primary reflectance and the active area primary reflectance, integrated over the AM1.5g spectrum in the range of 1000-1200 nm.

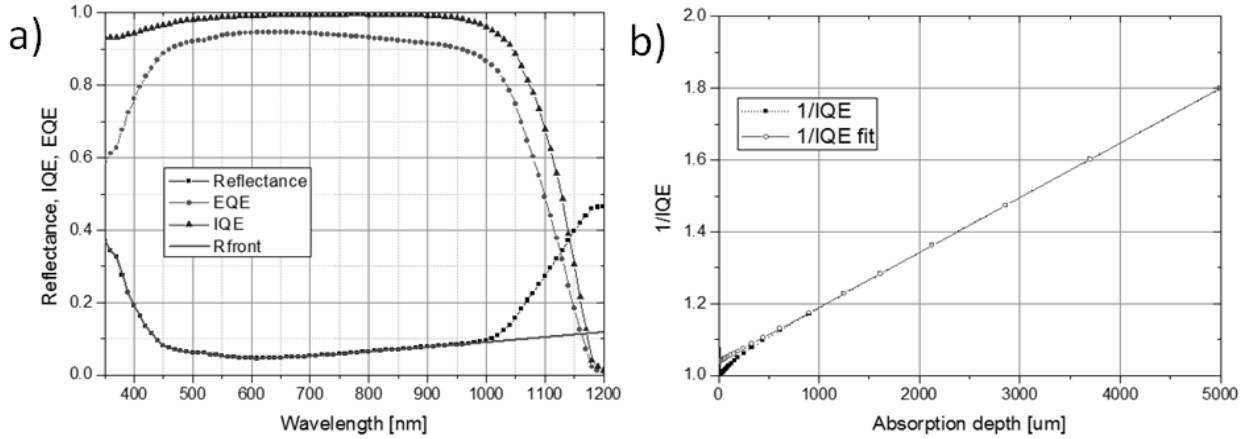


Figure 6.2. (a) IQE, EQE, Reflectance, and primary front reflectance (R_{front}) of the entire cell (including busbars). (b) Inverse IQE versus absorption depth. The linear 1/IQE fit is performed between 1000 and 5000 µm (i.e. for wavelengths between 1070 and 1120 nm).

From the results given in Table 6.2, the front grid shading loss currently accounts for 1.62 mW/cm^2 which represents more than 50% of the total optical losses. Thus, the easiest way to reduce optical losses for this device is to optimize the front grid design.

Table 6.2. Components of the optical losses and corresponding absolute power loss

parameter	front surface escape (+)	front grid shading loss only	front surface reflectance (++)	total
Optical losses [mA/cm^2]	0.63	2.34	1.34	4.32
Power loss [mW/cm^2]	0.44	1.62	0.93	2.99

[+] Calculated from the active area reflectance in the wavelength range of 1000-1200 nm.

[++] Calculated from the active area primary reflectance in the wavelength range of 300-1200 nm.

The specific contact resistance to the emitter was measured using transfer length method (TLM) test structures diced from the finished cell. The specific contact resistance to the BSF was measured on TLM structures typically used for the interdigitated back-contact solar cells. Using these values and knowing the front grid design (emitter R_{sh}=120 Ω/sq, finger pitch = 1 mm, ps-laser opening width=12 μm, plated Cu thickness=10 μm), the bulk parameters (thickness= 160 μm, resistivity = 2 Ω.cm), and the rear design (ns-UV laser diameter = 60 μm, dot pitch=600 μm); the individual series contributions can be calculated using the numerical formulas given in Chapter 3. All series resistance components are summarized in Table 6.3. From these results, optimization of the bulk parameters (resistivity vs. bulk lifetime) and of the emitter profile (contact resistance vs. recombination/current losses) could be envisaged.

Table 6.3. Components of the series resistance and corresponding absolute power-loss.

parameter	bulk	front fingers	contact emitter	contact BSF	emitter	total calculated	total measured
r_s losses [Ω.cm^2]	0.26	0.12	0.1	0.02	0.10	0.60	0.60
Power loss [mW/cm^2]	0.34	0.16	0.13	0.02	0.13	0.80	-

The different recombination mechanisms (bulk SRH, surface SRH, emitter, etc.) can be compared to one another by calculating the equivalent recombination current densities as proposed by Verlinden et al. [VER12c]. This requires to determine the excess carrier density in the device which can be calculated using linear approximations if the minority carrier current flow is: i) one dimensional and ii) follows a constant gradient from top to bottom of the cell. However, as explained by Kimmerle et al. [KIM12], both conditions (i) and (ii) are not valid for front junction PERC type solar cells. Therefore, in a first approximation, the total j_{sc} loss due to recombination (0.76 mW/cm^2) was calculated from the difference between the power loss due to the non-maximum value (3.75 mW/cm^2, see Table 6.1) and the total optical loss (2.99 mW/cm^2, see Table 6.2). Similarly the FF loss due to recombination (1.33 mW/cm^2) was obtained from the difference between the power loss due to the non-maximum value (2.14 mW/cm^2, see Table 6.1)

and the sum of the power loss contributions from series (0.80 mW/cm^2, see Table 6.3) and shunt resistances (0.01 mW/cm^2, see Table 6.4).

From the results summarized in Table 6.4, it appears that the largest power losses in the cell are due to recombination losses at V_{oc} (3.35 mW/cm^2), followed by optical losses (2.99 mW/cm^2), and recombination losses due to non-ideal n factor (1.33 mW/cm^2).

Table 6.4. Power loss analysis for the best 12.5x12.5 cm2 p-type i-PERC cell in this thesis

Loss	Optical losses [mW/cm^2]	Recombination losses [mW/cm^2]	r_s losses [mW/cm^2]	r_{sh} losses [mW/cm^2]	Total [mW/cm^2]
j_{sc} loss	2.99	0.76	-	-	3.75
V_{oc} loss	-	3.35	-	-	3.35
FF loss	-	1.33	0.80	0.01	2.14
Total power loss	2.99	5.44	0.80	0.01	9.24

Recombination losses at V_{oc} can be broken down into individual recombination losses based on individual dark saturation current density (J_0) contributions. Individual J_0 contributions are typically obtained from quasi-steady-state photoconductance-calibrated photoluminescence (QSSPC-PL, BTImaging) measurements on dedicated test wafers.

The passivated emitter $j_{0e,pass}$ was extracted from QSSPC-PL, after firing, using two side textured wafers with emitter and emitter passivation stack (thermal oxide/PECVD SiN_x) on both sides. The $J_{0e,metal}$ of the emitter contacted areas was extracted from Suns-Voc measurements on cells with varying front contact fractions as proposed by Fellmeth et al. [FELL11]. Knowing the front contact area A_{cont}, the quantities $j_{0e,pass}$ and $j_{0e,metal}$ can be related to total emitter j_{0e} according to the equation:

$$j_{0e} = j_{0e,pass} * (1 - A_{cont}) + j_{0e,metal} * A_{cont} \quad (6.6)$$

The effective rear surface recombination velocity $S_{rear,pass}$ was extracted by QSSPC-PL, after firing, on double side polished wafers featuring the rear passivation stack on both sides (thermal oxide/ PECVD SiO_y/SiN_x). Using the same double side polished wafers, a lower limit for the bulk lifetime τ_{bulk} was estimated from the measured effective lifetime at 1 sun. Finally, the rear surface recombination velocity at the metallized areas $S_{rear,BSF}$ was obtained by fitting long wavelength IQE results in PC1D for various rear contact pitches as described by Vermang et al. [VER12b]. The base dark saturation current density:

$$j_{0b} = \frac{q \cdot D \cdot n_i^2}{N_{dop} * L_{eff}} \quad (6.6)$$

is calculated from the elementary charge *q*, the minority carrier diffusion constant *D*, the intrinsic carrier concentration n_i, and the base doping density N_{dop}. A general definition of the effective diffusion length [WOL10] reads:

$$L_{eff} = L\frac{1+\frac{S_{eff}L}{D}\tanh\left(\frac{W}{L}\right)}{\frac{S_{eff}L}{D}+\tanh\left(\frac{W}{L}\right)} \quad (6.7)$$

with $L = \sqrt{D * \tau_{bulk}}$ (6.8)

which involve the bulk lifetime τ_{bulk}, the device thickness *W*, and the effective SRV at the rear surface S_{eff}.

As mentioned by Wolf and coworkers [WOL10], the literature provides several models that can be used to calculate S_{eff} from the measured $S_{rear,pass}$ and $S_{rear,BSF}$. In this work, we applied Fischer's model (see [WOL10] for detailed equations). To enable comparison of all recombination losses at V_{oc}, recombination velocities at the rear surface where converted into individual J_0 contributions according to the following equations:

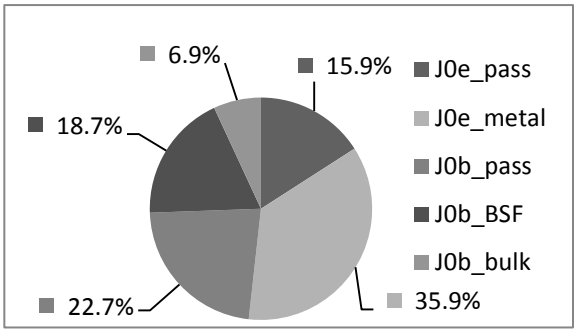
$$j_{0b,pass} = (j_{0b} - j_{0bulk}) * (S_{rear,pass} / S_{eff}) \quad (6.9)$$

$$j_{0b,pass} = (j_{0b} - j_{0bulk}) * (1 - S_{rear,pass} / S_{eff}) \quad (6.10)$$

where J_{0bulk} is calculated using equation (6.6) and assuming S_{eff} is zero in equation (6.7). Measured values and corresponding individual J_0 contributions given as percentage of the total J_{01} (calculated from V_{oc} using the 1 diode equation given in Chapter 2) are summarized in Table 6.5.

Table 6.5. Measured cell parameters and corresponding individual J_0 contributions in percentage of total J_{01}.

location	Passivated area	Contacted area	contact fraction
emitter	$J_{0e,\ pass}$=40 fA/cm^2	$J_{0e,\ metal}$=2500 fA/cm^2	3.48%
bulk	τ_{bulk} =2 ms	-	-
Rear surface	$S_{rear,pass}$=27 cm/s	$S_{rear,metal}$=1700 cm/s	1.48%



Recombination losses at V_{oc} are found to be mainly limited by the high recombination under the front contacts (35.9%) followed by recombination due to the rear passivation and the rear BSF regions (22.7% and 18.7% respectively). The high recombination under the front contacts can be understood by the fact that the chosen 1 µm deep homogeneous 120 Ω/sq emitter is highly sensitive to minority carrier recombination at the surface (see Chapter 4.1) leading to high $J_{0e,metal}$ values. Thus, possible ways to reduce $J_{0e,\ metal}$ include: i) optimize front laser ablation to reduce laser damage, ii) optimize emitter profile (higher surface concentration) to provide better shielding of the contacts without compromising $J_{0e,pass}$, or iii) implement a selective emitter structure as evidenced by Fellmeth et al. [FELL11].

Using PC1D simulations [BAS88] and starting from our best cell on 12.5x12.5 cm^2 (η=20.5%), we have estimated efficiency improvements due to possible cell design and process changes. From the results given in Table 6.6, increasing the front finger pitch from 1 mm to 1.25 mm (scenario A) to reduce grid shading down to 4.1% should be readily implemented as it presents the potential for +0.3% absolute gain in efficiency. Optimization of the front grid design was implemented when transferring the process to 15.6x15.6 cm^2 and efficiencies up to 20.8% could be confirmed (see Chapter 5.4.3). Following this, reducing the effective rear surface recombination velocity S_{rear} from 52 cm/s down to 30 cm/s (scenario A+B) would lead to another +0.3%abs. gain leading to eta>21%. This could possibly be achieved by introducing Al_2O_3 passivation to reduce $S_{rear,pass}$ from the current 27 cm/s down to 10 cm/s [VER12b]. Al_2O_3 passivation is currently being investigated at imec together with Ni/Cu/Ag plated contacts. Improving the backside reflectivity from 95% to 98% would also lead to eta>21% (scenario A+C). The impact of rear metallization of back side reflectance is quickly introduced in section 6.2.6. As mentioned before, another area of improvement requires reducing the recombination under the front contacts $j_{0e,metal}$. Going from $j_{0e,metal}$ =2500 fA/cm^2 down to $j_{0e,metal}$ =1250 fA/cm^2 would give another +0.3% gain (scenario A+D). This could possibly be done by implementing laser doped selective emitters as discussed by Wang et al. [WAN12]. Finally, combining all possible improvements (A+B+C+D) we estimate efficiencies up to 21.5%.

Table 6.6. Input parameters used for PC1D simulations and resulting I-V results for different cell designs. Input values for the reference cell are taken from Tables 6.3 and 6.5, the external front reflectance R_{front} is taken from the experimental data (Figure 6.2a). All simulations were performed with: ρ=2 Ω.cm, τ_{bulk} =2 ms, internal diode: $7x10^{-9}$ A/cm^2, n_i=9.6510^9 cm^{-3} at 300K [WOL10].

		Reference	A	A+B	A+C	A+D	A+B+C+D
emitter contact	[$\Omega.cm^2$]	0.34	0.44	0.44	0.44	0.44	0.44
S_{front}	[cm/s]	6100	5000	5000	5000	3500	3500
S_{rear}	[cm/s]	52	52	30	53.6	52	30
front shading	[%]	5.7	4.1[#]	4.1	4.1	4.1	4.1
R_{front}, internal (diffuse) 1st/subsequent bounce	[%/%]	94/94	94/94	94/94	94/94	94/94	94/94
R_{rear}, internal (specular) 1st/subsequent bounce	[%/%]	94/92	94/92	94/92	99/97[##]	94/92	99/97
simulated jsc	[mA/cm^2]	38.6	39.2	39.3	39.7	39.3	39.8
simulated Voc	[mV]	665.1	668.4	674.9	668.7	673.1	678.6
simulated FF	[%]	79.9	79.4	79.4	79.4	79.4	79.6
simulated eta	[%]	20.5	20.8	21.1	21.1	21.1	21.5

[#]Reflectance R_{front} obtained by averaging 4 cm^2 measurements over busbars and fingers to end up with 4.1% shading.
[##]Equivalent to total reflectance at 1200 nm R_{total}=70% which could be achieved using the same passivation stack but avoiding Al firing leading to an internal backside reflectance ρ~98%. Further discussed in section 6.2.6.

6.2. Optimization of standard solar cell processing steps

6.2.1. Front emitter profile

As discussed in Chapter 4, homogeneous front-side emitters in p-type silicon solar cells can be formed using a wide variety of techniques ($POCl_3$ diffusion, inline diffusion, implantation, etc.). Due to the contact resistance and line width limitations of silver screen printed contacts, front emitter profiles used in industry typically feature high surface dopant concentrations ($N_s > 1x10^{20}$ at/cm^3) and sheet resistances ~60-100 Ω/sq. Front emitter profiles are optimized to minimize the amount of inactive phosphorous dopants ("dead-layer") that are present close to the surface. On the other hand and as discussed in Chapter 5, Ni/Cu/Ag plated contacts offer low specific contact resistance down to $Ns \sim 1x10^{19}$ at/cm^3 together with narrow contact widths thanks to self-aligned nature of plating. Thus, an optimization of the front emitter profile is required when replacing Ag screen printed contacts by Ni/Cu/Ag plated contacts.

The optimization of the front homogeneous emitter profile for Ni/Cu/Ag plated contacts is quite challenging, particularly for a simplified plating sequence where sintering is performed at the end, since it requires to find compromises between:

- recombination losses in the emitter bulk and at the passivated surface
- recombination losses under the front metal contacts
- optical losses in the emitter
- resistive losses (in particular contact resistance losses)
- recombination losses in the space charge region (i.e. junction damage caused by laser ablation and/or Ni, Cu diffusion during sintering)
- long-term reliability (deeper emitters might be more robust to metal in-diffusion)
- cost-of-ownership (high temperature oxidations required to form deep emitters might be too costly for industrial implementation)

The strategy followed during this thesis for emitter optimization was to first develop this simplified plating sequence on a robust deep emitter and then evaluate it on simpler, less deep, emitter profiles. Target emitter profiles can be defined from literature by superimposing the passivated emitter dark current saturation density (i.e. $j_{0e,pass}$) contour plot with the sheet resistance contour plot as shown in Figure 6.3a. Resistive losses due to lateral current in the emitter and front grid shading losses limit emitter sheet resistances to the range of 100-150 Ω/sq. Moving away from a typical 60-100 Ω/sq industrial emitter profile featuring N_s (profile A) and limiting ourselves to $N_s \geq 1x10^{19}$ cm^{-3}, we can define the first target profile as having $N_s \sim 1x10^{19}$ cm^{-3} and a junction depth (x_j) of 1 µm (profile B). Emitter profiles C ($N_s \sim 4x10^{19}$ cm^{-3}, $x_j \sim 0.5$ µm) and D ($N_s \sim 4x10^{19}$ cm^{-3} $x_j \sim 0.5$ µm) could then be evaluated as they are potentially cheaper to manufacture. As mentioned in Chapter 4, emitter profile B yields the highest efficiency potential provided surface passivation schemes offering low surface recombination velocity are used. As evidenced in Figure 6.3b, thermal oxide passivation in combination with an hydrogenation step (e.g. FGA anneal or PECVD SiN_x + firing) is preferred over PECVD SiN_x passivation only.

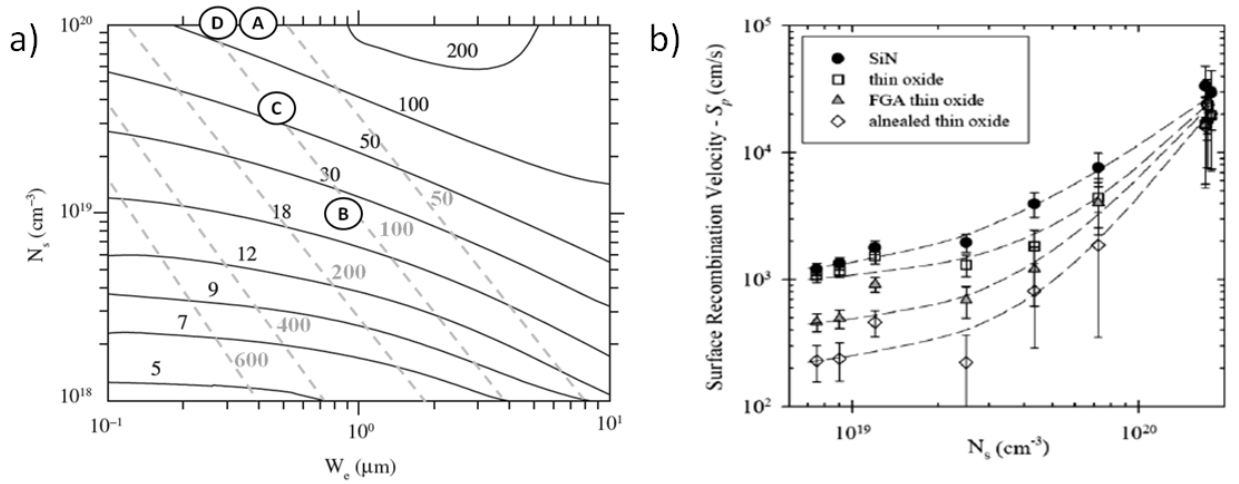


Figure 6.3. (a) Solid lines: passivated emitter dark current saturation density, $J_{0e,pass}$ (fA/cm^2), as a function of surface doping concentration, $N_{s,}$ and junction depth, W_e. [SAN09]. Dashed lines: emitter sheet resistance (Ω/sq) of Gaussian n-type emitters as a function of N_s and W_e [CUE00]. (b) Surface recombination velocity for different passivation schemes as a function of surface phosphorous doping concentration on planar <100> FZ-Si [KER02].

Emitter profiles used in this thesis are based on a two-step approach. In a first step, a shallow profile is formed by $POCl_3$ diffusion and the phosphorous silicate glass (PSG) is removed by wet chemistry (HF dip). In a second step, a thermal oxidation is performed to drive-in dopants deeper in silicon and passivate the surface with a thin thermal oxide. Since the source of dopants is removed prior to thermal oxidation, the surface concentration is effectively reduced while the junction depth increases. In the standard i-PERC sequence (see Figure 6.1), additional wet chemistry steps are present between PSG removal and thermal oxidation. These steps are rear inline emitter removal and wafer cleaning. Since they result in some etching of doped silicon, they can considerably affect the emitter profile prior to thermal oxidation and hence the final emitter profile. In particular, NO_x vapors generated during rear inline emitter removal in $HF/HNO_3/H_2SO_4$ can lead to a considerable increase in sheet resistance at the front side even though it is not in contact with the etching solution [COR12]. Alternative integration routes (rear diffusion mask prior to $POCl_3$ or rear emitter removal performed after the high temperature oxidation) have also been evaluated during the course of thesis and results are discussed elsewhere [NGA12]. For a given starting profile, the final profile shape can be tailored by the parameters used for thermal oxidation (temperature, duration, gas flows, ramp rates, etc.). Simulation tools exist, such as Sentaurus sprocess [SYN12], that can accurately simulate the emitter profile after thermal oxidation. An example of such simulations is shown in Figure 6.4a where all thermal oxidation parameters were the same except the annealing temperature. From these simulations, it becomes clear that high temperature oxidations, which are not desired for industrial high-throughput production, are required to achieve deep junctions. In addition, such high temperature oxidation might lead to considerable degradation in bulk lifetime. This aspect is further discussed in section 6.1.2. However, industrial alternatives to form relatively deep emitters do exist. For instance, a heavy $POCl_3$ diffusion can result in a relatively deep junction

thanks to the phosphorous "push-effect" [BEN06] and a subsequent emitter etch-back can be performed prior to low temperature oxidation to obtain the desired R_{sh}, N_s values [LAC12]. Industrial solutions have also been proposed to perform long oxidations without compromising throughputs [HOR09b]. Recently, progress has been made in developing accurate models for the more complex $POCl_3$ diffusion process [SCH13]. Such process simulations can then be combined with device simulations to determine the $POCl_3$ diffusion (and thermal oxidation) parameters leading to the optimum emitter profile. However, the presence of intermediate wet chemistry steps is still a source of discrepancy between simulated and measured emitter profiles. Therefore, in this thesis emitter profile optimization was based on experimental data.

Various homogeneous emitter profiles, which are given in Figure 6.4b, were developed and investigated in this thesis. These profiles correspond fairly well to profiles C to D described earlier and can be compared with a standard 80 Ω/sq profile (similar to profile A) typically used with screen printed Ag contacts at imec [PRA12]. The thermal oxidation temperature and duration at peak temperature used to obtain these profiles are also mentioned in Figure 6.4b. It should be mentioned that to obtain these profiles not only the thermal oxidation parameters were changed but also the $POCl_3$ diffusion parameters. The front thermal oxide thickness was optimized to minimize optical losses and parasitic plating. These two aspects are further discussed in section 6.1.3. Solar cells results obtained for these various profiles are discussed below while long-term reliability results with Ni/Cu/Ag plated contacts are presented for two of these profiles (80 Ω/sq and 130 Ω/sq 1 µm deep) in Chapter 7.

Large area (15.6x15.6 cm^2) p-type, 1-2 Ω.cm, m-CZ-Si wafers were processed into i-PERC solar cells using the sequence given in Figure 6.1. Front side metallization was performed using the simplified Ni/Cu/Ag plating sequence in the MECO plating tool and subsequent sintering for 4min at 250˚C in the BTU VMCA tool. Test wafers were co-processed to monitor changes in emitter dark current saturation density $J_{0e,pass}$ (extracted from QSSPC-PL at $1x10^{16}$ cm^{-3} injection level) during processing.

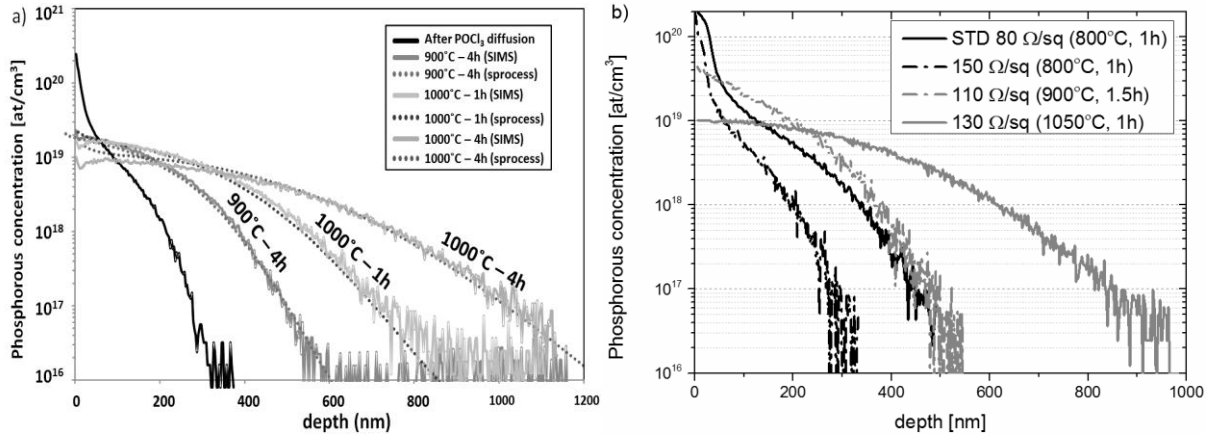


Figure 6.4. (a) Example of measured starting $POCl_3$ profile (SIMS) and simulated (SENTAURUS sprocess) phosphorous profiles after various thermal oxidations. (b) SIMS profiles of emitters used in this work. Measured sheet resistances values and thermal oxidation parameters (peak temperature and duration at peak temperature) are given as reference. Thermal oxide was removed prior to SIMS measurement.

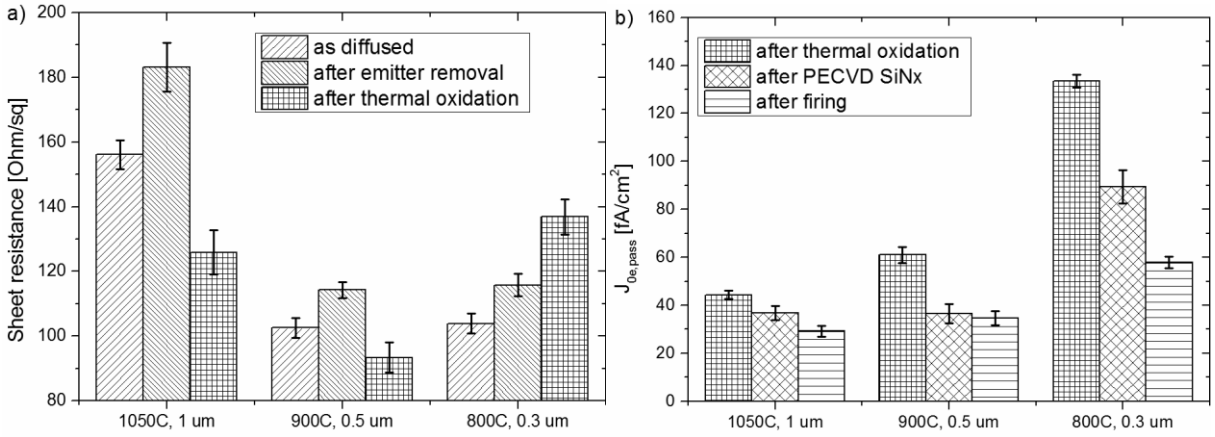


Figure 6.5. (a) Measured sheet resistance values (64 points per wafer) for the different emitters at various processing stages. (b) Passivated emitter dark current saturation density, $J_{0e,pass}$ (fA/cm^2), extracted from QSSPC-PL on double side textured p-type m-CZ-Si wafers, for the different emitters at various processing stages. In both graphs, results are averaged over 3 wafers. A Tempress direct PECVD system was used for SiN_x deposition. Firing was performed in belt furnace for a couple seconds at ~800˚C (wafer temperature).

The rear inline emitter removal is found to induce large increase (up to 25 Ω/sq) in front side emitter sheet resistance as shown in Figure 6.5a. This is particularly problematic for the 1 µm and the 0.3 µm deep emitters since the starting $POCl_3$ profile are relatively shallow. As mentioned before, NO_x vapors generated during Si etching are responsible for this increase. Therefore exhaust, solution temperature, and number of wafers in the bath should be kept well under control as they were found to have a large impact on the measured sheet resistance increase and its variation within wafer [COR12]. Sheet resistances lowered upon high temperature oxidation while they increased upon low temperature (800˚C) oxidation which can be understood as follows. At low temperature, inactive (and active) dopants close to the surface are consumed faster by oxide growth than they are driven-in and hence the sheet resistance increases. For high temperature oxidation, the opposite behavior is happening which has significant implications on the amount of phosphorous incorporated in the thermal oxide as discussed in section 6.1.4. Such behaviors might strongly differ depending on the starting $POCl_3$ profile and the oxidation parameters (e.g. oxidation performed prior to or after drive-in in N_2). Finally, slight modifications were made to the starting $POCl_3$ profiles so that in the solar cell run, all three emitters would result in sheet resistances in the range of 100-130 Ω/sq.

Interestingly, passivated emitter dark current saturation density values ($j_{0e,pass}$~35 fA/cm^2, see Figure 6.5b) measured after PECVD SiN_x deposition and firing for the 0.5 µm deep emitter are only slightly higher than with the 1 µm deep emitter ($j_{0e,pass}$~30 fA/cm^2). Further optimization of the front PECVD SiN_x to obtain lower surface recombination velocities could possibly result in a larger difference in favor of the 1 µm deep emitter. For the 0.3 µm emitter, measured values ($j_{0e,pass}$~58 fA/cm^2) are on a good level compared to simulated literature data (see Figure 6.3a) but still much higher than for the other two emitters and hence lower open-circuit voltage values (V_{oc}) are expected.

Table 6.7: Average (over 6 cells) electrical parameters for large area (15.6x15.6 cm^2) i-PERC solar cells processed in the MECO plating and BTU sintering tools using the simplified sequence for Ni/Cu/Ag contacts (front grid design: 3 busbars, 1 mm finger pitch). Some groups were processed in different direct PECVD systems which are mentioned (CENT: Centrotherm, TEMP: Tempress). The group featuring the 0.3 µm emitter was plated separately and hence the busbar-to-busbar resistance (R_{bb}) is lower due to reduced plated Cu thickness. All three emitter profiles gave sheet resistances in the range of 100 to 130 Ω/sq.

Emitter profile	PECVD	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	ŋ [%]	r_s [$\Omega.cm^2$]	n	pFF [%]	R_{bb} [mΩ]
1050˚C, 1 µm	CENT	38.9	645.5	77.9	19.5	0.88	1.07	82.7	14.5
900˚C, 0.5 µm	CENT	38.8	642.6	78.4	19.6	0.78	1.07	82.7	18.3
900˚C, 0.5 µm	TEMP	39.4	655.5	78.4	20.2	0.72	1.10	82.5	17.2
800˚C, 0.3 µm	TEMP	39.4	644.5	76.3	19.4	1.02	1.16	81.7	25.2

Average I-V illuminated results obtained with the different emitters are presented in Table 6.7 together with some other electrical parameters. Unfortunately, direct comparison between all three emitters is not possible since the PECVD depositions (front SiN_x and rear SiO_y/SiN_x) where done in different systems for availability reasons. Using the same PECVD system, the 0.5 µm deep emitter yields comparable results as the 1 µm deep emitter. The identical pseudo fill factors (pFF) values demonstrate that the 0.5 µm deep emitter can withstand junction damage induced by laser ablation and/or during sintering of the full Ni/Cu/Ag stack. The comparable short-circuit densities (j_{sc}) are confirmed by internal quantum efficiency (IQE) with both emitters giving the same response at short wavelengths (see Figure 6.6a). For the 0.5 µm deep emitter, we attribute the higher fill factors (FF) values to lower contact resistance values (confirmed in Figure 6.8a) since the grid design is identical (same finger pitch, similar emitter R_{sh}), R_{bb} (busbar-to-busbar resistance) values are higher, and pFF values are comparable. For the same emitter depth, solar cells processed in the Tempress system gave higher V_{oc} and j_{sc} values as compared to cells processed in the Centrotherm system. Based on IQE measurements (see Figure 6.6a), we attribute these differences to both improved front and rear surface passivation. Finally, cells featuring a 0.3 µm deep emitter and Tempress PECVD dielectrics gave lower FF and V_{oc}. Consequently, average efficiencies dropped from 20.2%, for the 0.5 µm deep emitter, down to 19.4%. The lower FF values are attributed to both higher series resistance due to insufficient Cu plating (higher R_{bb}) and increased junction damage as shown by the fact that pFF values dropped below 82%. IQE measurements did not reveal any difference at short wavelengths between the two emitters that could explain the lower V_{oc} values (see Figure 6.6b). Only a minor gain in IQE is visible at short-wavelength compared to a 80 Ω/sq emitter ($j_{0e,pass}$~180 fA/cm^2) typically used in combination with screen printed Ag contacts [PRA12]. It is speculated that recombination under the laser ablated and plated contacts is limiting the short-wavelength response of those cells since measured $J_{0e,pass}$ were considerably lower (see Figure 6.5b). Differences is reflectance at short wavelength are further discussed in section 6.1.4.

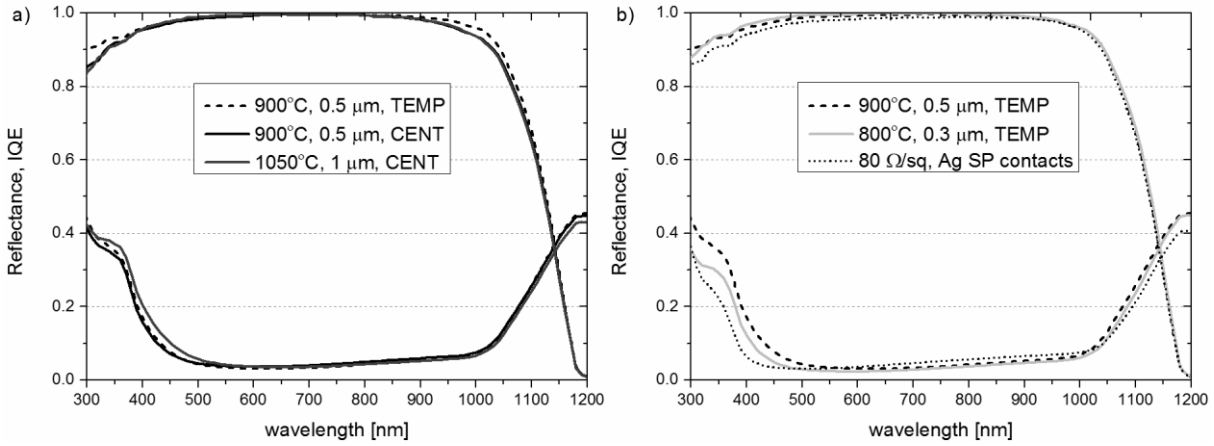


Figure 6.6. (a) Internal quantum efficiency (IQE) and reflectance curves for two different emitter profiles and two different PECVD deposition systems (details in text) (b) IQE and reflectance curves for two different emitter profiles (details in text) for the same PECVD deposition system. IQE and reflectance curves of typical i-PERC solar cell featuring a 80 Ω/sq emitter (shown in Figure 6.4b) and screen printed Ag contacts, are given as reference.

For the present 0.3 µm deep emitter, both the drop in V_{oc} and in pFF can be attributed to emitter surface and bulk damage caused during ps-UV laser ablation of the front dielectrics. This is demonstrated from Suns-Voc measurements, given in Figure 6.7, where both Suns-Voc and pFF values drop with increased laser power even before sintering of the full Ni/Cu/Ag stack is performed. Using "softer" ablation conditions is not possible as this would compromise adhesion (see Chapter 7). As discussed in Chapter 5, damage-free ablation of dielectrics is challenging on alkaline textured surfaces due to interference effects at the pyramid tips and edges. Interference effects possibly lead to defects locally extending as deep as 0.3 µm that get decorated during plating and hence could explain the low pFF values measured before sintering. Controlled etching experiments recently published by Gall et al [GAL13] indicated that defects generated during ps-UV ablation can extend even deeper than 0.3 µm. Such defect etching evaluations are being started at imec and are the focus of another PhD thesis.

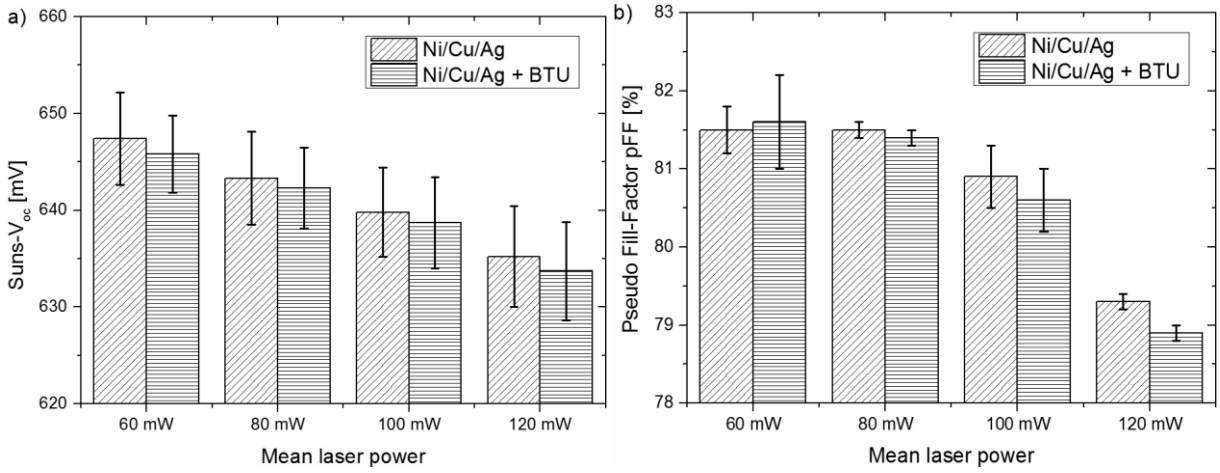


Figure 6.7. (a) Suns-Voc and (b) pseudo fill factors measured on mini i-PERC cells (area 5x5cm^2) featuring a 0.3 µm deep emitter for various ps-UV laser conditions before and after sintering in the BTU tool for 4 min at 250°C.

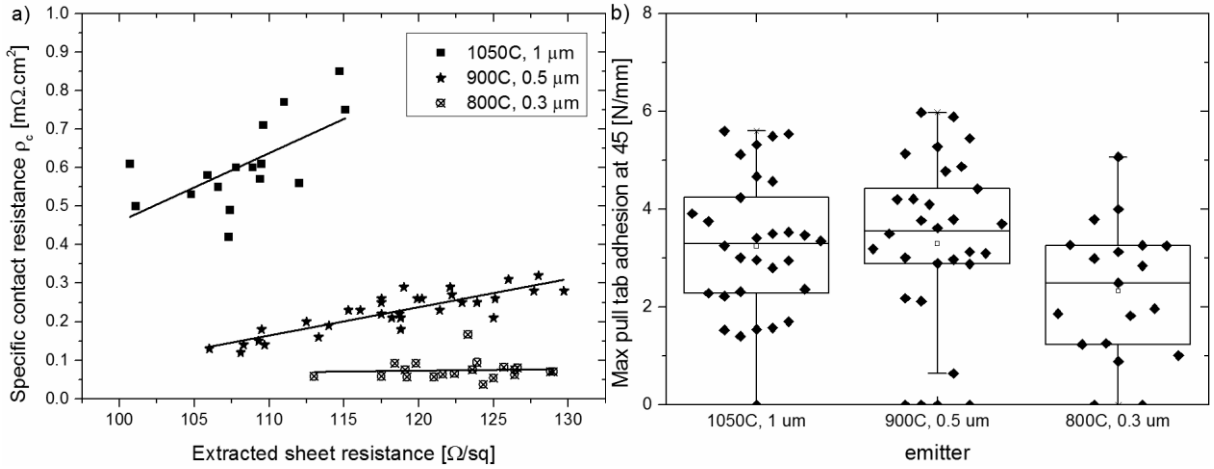


Figure 6.8. (a) Measured specific contact resistance vs. extracted sheet resistances obtained from TLM measurements on finished devices for various emitter profiles. (b) Adhesion results for the same profiles.

In this section, average efficiencies of 20.2% could be demonstrated on large area (15.6x15.6 cm^2) i-PERC devices using a 0.5 µm 100-130 Ω/sq deep emitter and a simplified Ni/Cu/Ag plating sequence. This emitter was shown to lead to comparable results as with a high-efficiency 1 µm emitter. In addition, specific contact resistance measurements (see Figure 6.8a) confirmed that, due to its higher surface concentration, the 0.5 µm emitter is more robust to variations in emitter sheet resistance which are induced during processing ($POCl_3$ diffusion, emitter removal, pre-oxidation cleaning). These results were obtained without changing the parameters used for front ps-UV laser ablation and hence comparable pull adhesion values (average >3N/mm) could be demonstrated (see Figure 6.8b). Going further, results on a 0.3 µm 100-130 Ω/sq shallow emitter were found to be mainly limited by emitter surface and bulk damage created during ps-UV laser ablation of the front side dielectrics and not by diffusion of Ni and/or Cu during the final sintering step. Further optimization of laser ablation (e.g. testing different pulse durations) or the implementation of laser doped selective emitters might enable the use of such shallow emitters in combination with Ni/Cu/Ag contacts. This could be the focus of future research. Finally and as mentioned at the beginning of this section, long-term reliability results should also be demonstrated before defining a 0.5 µm 100-130 Ω/sq deep emitter as being close to the optimum profile. Long-term reliability aspects are discussed in Chapter 7.

6.2.2. CZ-Si material influence

The simplified Ni/Cu/Ag plating sequence developed in this thesis on p-type monocrystalline wafers benefits from high temperature processing and emitters that are collecting minority carriers created in all parts of the device (including short wavelengths). This is fundamentally different than with p-type solar cells featuring screen printed Ag contacts where processing is generally kept below 900˚C and the top-most region of the emitter, which is electrically inactive (so-called "dead-layer), can be used to getter harmful metallic contaminants.

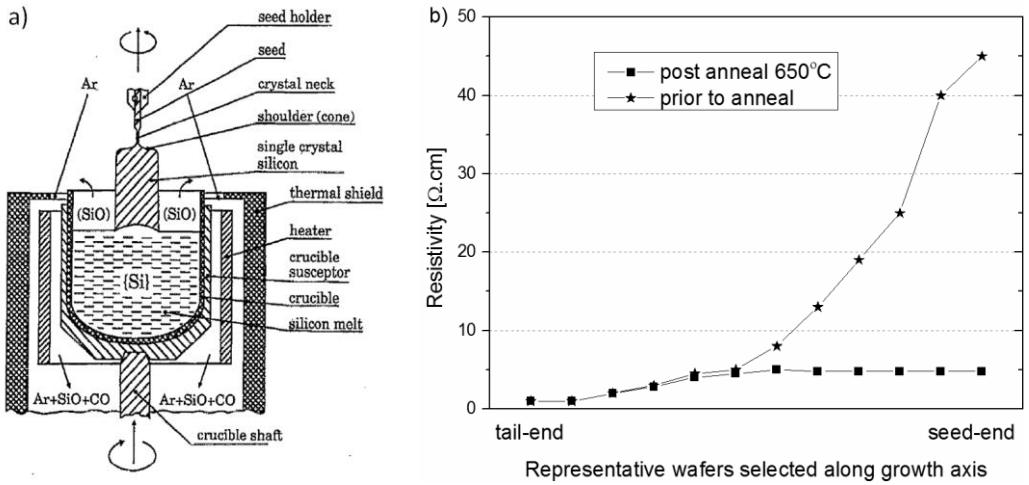


Figure 6.9. (a) Schematic of ingot pulling during Czochralski (CZ) process. Taken from [BOR95]. (b) Resistivity of gallium doped CZ-Si wafers, taken along the ingot, prior to and after thermal donor anneal at 650˚C for 30min.

Good knowledge of defects present in as-grown monocrystalline silicon and their evolution during processing is required to benefit fully from this simplified Ni/Cu/Ag plating sequence. At present, the majority of monocrystalline silicon solar cells are made from wafers that are wire-sawn from ingots grown using the Czochralski (CZ) process. In this process, a precisely oriented rod-mounted seed crystal is dipped into high-purity silicon that is molten in a crucible. A single-crystal silicon ingot is then formed by slowly pulling upwards and rotating the seed crystal's rod as shown in Figure 6.9a. If not suppressed, melt convection flows transport oxygen that is dissolved at the quartz crucible walls into the melt and result in the incorporation of ~10^{18} cm^{-3} of interstitial oxygen in the CZ-Si ingot. This level of oxygen is supersaturated below ~1200˚C, so the equilibrium state is reached by the formation of SiO_2 particles (oxide precipitates) [BOR95]. Parameters like growth speed, ingot rotation rate and crucible rotation speed as well as cooling rate have a strong influence on the distribution of oxide precipitates along the ingot axis and perpendicular to it [HOR12 and references therein]. As they grow, these precipitates can become strained and eventually be surrounded by extended defects such as dislocations or stacking faults [BER89]. The formation of all these defects and their interaction with other impurities (dopants, metallic impurities, etc.) is an issue for solar cell processing. In this section their influence is described based on whether they are thermal-donors, oxide precipitates, or boron-oxygen complexes.

Regions of the CZ-ingot with high oxygen concentrations typically have high concentrations of electrically active thermal donor states [BOR95]. This is because cooling a 200 mm diameter ingot is much too slow to prevent thermal donor formation. The concentration of electrically active thermal donors can be drastically reduced by applying a low temperature anneal [BOR95]. This is shown in Figure 9b, where the base resistivity was measured on gallium doped wafers selected along the ingot length before and after applying a thermal anneal at 650˚C for 30min. The measured gradient in resistivity along the ingot length is for big parts due to oxygen concentration rather than to the low segregation coefficient of Ga. Seed-end regions

typically have a considerably higher O_i concentration that center or tail-end regions [BOR95]. This can be understood as follows. At the beginning of the pulling process, large quantities of O_i are taken from the melt. As pulling progresses, O_i incorporation reduces because oxygen evaporates from the melt surface and the area in contact with the crucible gets smaller compared to the evaporating surface. The measured thermal donor states in as-cut wafers is not an issue as they will typically mostly disappear during solar cell processing. However, if not de-activated they might lead to erroneous lifetime measurements since accurate resistivity information is required. On the other hand, measuring changes in resistivity due to thermal donors along an incoming ingot is a simple way to detect which areas of the ingot have high O_i concentrations.

A high number of oxide precipitates can form or grow in size during high temperature processing depending on the thermal history (cooling rate, post-treatment to eliminate thermal donors performed by ingot manufacturer) and point defect concentrations in the CZ-Si material. Furthermore, high temperature processing (>900 ˚C) can lead to the dissolution of metal impurities present as metal precipitates in the starting CZ-Si material. Metal impurities might spread over wider regions or get partially trapped at oxide precipitates where they impact minority carrier lifetime. In fact, the recombination activity of dislocations surrounding oxide precipitates has been shown to be strongly enhanced by contamination with metallic impurities [KVE01, FEL93]. Extensive investigations recently published by Murphy et al. [MUR13] suggest that the recombination activity of oxide precipitates and surrounding defects is dependent on precipitate density (and not size) and is determined by the number of iron atoms (present in as-grown CZ-Si) decorating these defects. To illustrate the dependence of solar cell processing on the starting CZ-Si material, wafers from different ingots, with similar oxygen and boron doping concentrations but increasing metal concentrations, were treated in two different ways. After saw damage removal on both groups, an external pre-gettering ($POCl_3$ n^+ diffusion at ~840˚C) was applied on half of the wafers (group B). Subsequently, all wafers went through an i-PERC sequence featuring a 1 µm deep 120 Ω/sq emitter (see Figure 6.1). Minority carrier lifetime was assessed on device level with the exception that metal contacts and the subsequent firing step (local Al-BSF formation) were not yet applied. The firing step is known to improve the lifetime further (hydrogen release from PECVD SiN_x layers). From the lifetime results, given in Figure 6.10, it can be seen that without pre-gettering all these materials respond poorly to high temperature processing. The concentric ring or swirl-like patterns present on these lifetime maps have also been reported by other research groups [HAU11, KUL12, SON13]. Such patterns are related to differences in cooling rates during crystal growth leading to variations in point-defects concentrations (in particular vacancies) and hence in the concentration of (metal decorated) oxide precipitates that nucleated at those sites. Applying an external pre-gettering step, drastic improvements are obtained for wafers of material 1b and 2b. This is because metal impurities such as Fe are preferentially gettered in the n^+ regions, which were removed during texturing, than at the oxide precipitates [MUR13]. However, for material 3b, featuring a high metal concentration, no improvement could be observed with pre-gettering since a large portion of metal impurities is also being gettered internally at oxide precipitates and surrounding defects.

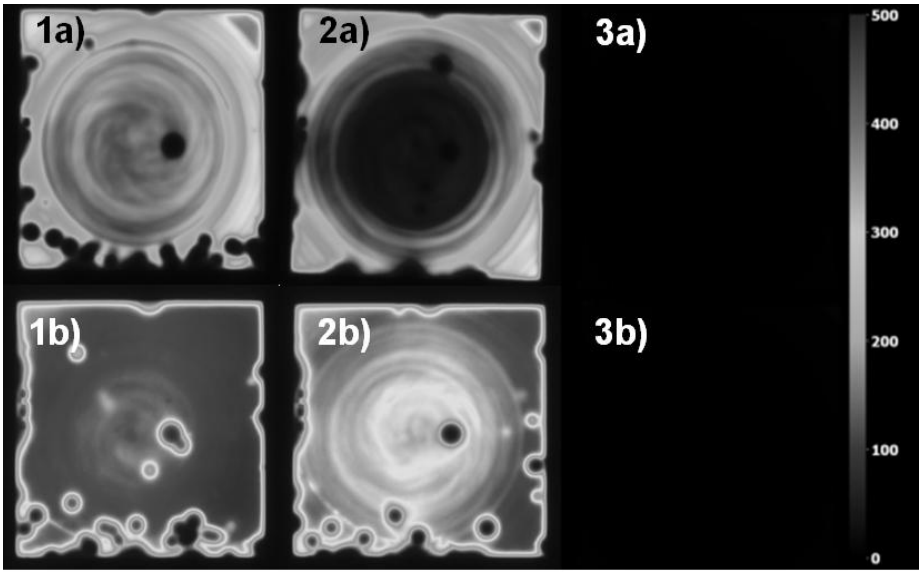


Figure 6.10. QSSPC calibrated photoluminescence (PL) effective lifetime images (scale 0 to 500µs) at 1e15cm^{-3} injection level for p-type CZ-Si material 1 to 3 without (a) and with (b) an external pre-gettering step.

Following these lifetime results, i-PERC solar cells were processed on these various p-type CZ-Si materials using either a shallow 80 Ω/sq in combination with screen printed (SP) Ag contacts or a 1 µm deep 120 Ω/sq emitter in combination with plated Ni/Cu/Ag. The Cu plated cells were shown to outperform the SP Ag cells if a pre-gettering step was applied and the results are further discussed elsewhere [HOR12]. Still it would be desirable to minimize metal impurity concentrations and to reduce internal gettering sites (i.e. oxide precipitates and surrounding defects). Internal gettering sites can possibly be reduced by adapting/controlling the cooling regime during crystal growth. Performing a heavy $POCl_3$ diffusion, a subsequent emitter etch-back, and low temperature oxidation as currently done by Schott Solar in their record PERC cells [LAC12, MET13] might also be a good strategy to implement external gettering and limit the nucleation and growth of internal gettering sites. Cost-effective implementation of external gettering are currently being investigated at imec in several solar cell architectures. Finally, reducing O_i incorporation during ingot growth is also a very effective way to prevent the formation of oxide precipitates. This can be achieved by using magnetic confinement (m-CZ-Si) to suppress Si melt convection flows during ingot pulling [MOS12]. With that type of growth, O_i concentrations could be drastically reduced from 7-12x10^{17} cm^{-3} down to 4x10^{17} cm^{-3} for most part of the ingot [HOR12]. Today, the cost for magnetic confinement of the melt is only part of the cost of a CZ-Si puller and can be compensated by faster growth rates and higher productivity. Results given in this thesis were obtained on m-CZ-Si unless mentioned otherwise.

A final point of attention with p-type CZ-Si material is boron-oxygen complexes which upon illumination lead to the phenomena referred to as light-induced degradation (LID) [VOR10, LIM10, LIM11]. LID can easily result in degradation in efficiencies by more than 1%$_{abs.}$ if no precautions are taken to minimize such losses. It is known that LID increases with increasing oxygen and boron doping concentrations. Recently, a post-treatment strategy to

permanently stabilized solar cells or modules at high efficiencies has been suggested in a patent by Herguth et al. [HER11]. Reducing O_i concentrations also proved to be very effective at reducing LID losses. In that respect, using the m-CZ-Si described earlier (O_i<4x10^{17} cm^{-3}) we could reduce LID losses to less than <-0.2%$_{abs.}$ without any post-treatment [HOR12].

6.2.3. Front ps-UV laser ablation

Initial developments of front dielectric(s) patterning on alkaline textured surfaces were performed using a Thrumph ns-UV laser marking system (λ= 355 nm, pulse duration~13 ns at 75Khz repetition rate) and are discussed in Chapter 5. Average efficiencies ~19.2%, equivalent to the ones obtained with a reference wet etch patterning process, were demonstrated using optimized conditions for the ns-UV laser ablation (5 µJ/pulse, 25% pulse overlap, ~20 µm line widths). However, it became quickly apparent that narrower line widths and more uniform ablation would be desirable to obtain higher efficiencies and ensure sufficient mechanical adhesion of the Ni/Cu/Ag plated contacts. Therefore, complete re-optimization of the front dielectric(s) patterning process was performed as a more advanced Talisker ps-laser platform from Coherent (pulse duration~12 ps at 200Khz) was installed at imec. All process developments were performed using ps-UV laser ablation as extended crystal defects were reported for the ablation of SiN_x layers on alkaline textured surfaces with ps-visible laser pulses (see Chapter 5).

Scanning electron microscope (SEM) images of ablated lines are considerably different with the Talisker ps-UV system. Instead of leading to pyramid melting and incomplete SiN_x (n=2.0) removal as with ns-UV ablation (see Figure 6.11a), ps-UV laser ablation is found to give narrow line widths (~8-10 µm) and more uniform ablation with ripple structures at the surface (Figure 6.11b). Narrower line widths are simply caused by better optics in the Coherent system while the ripples (or so-called laser induced periodic surface structures) have been described as the result of interference between the incident light and an electromagnetic surface wave [HER10b]. However, ps-UV ablation is found to be much less uniform in the case of a thermal oxide/PECVD SiN_x double anti-reflective coating (DARC) as shown in Figure 6.11c.

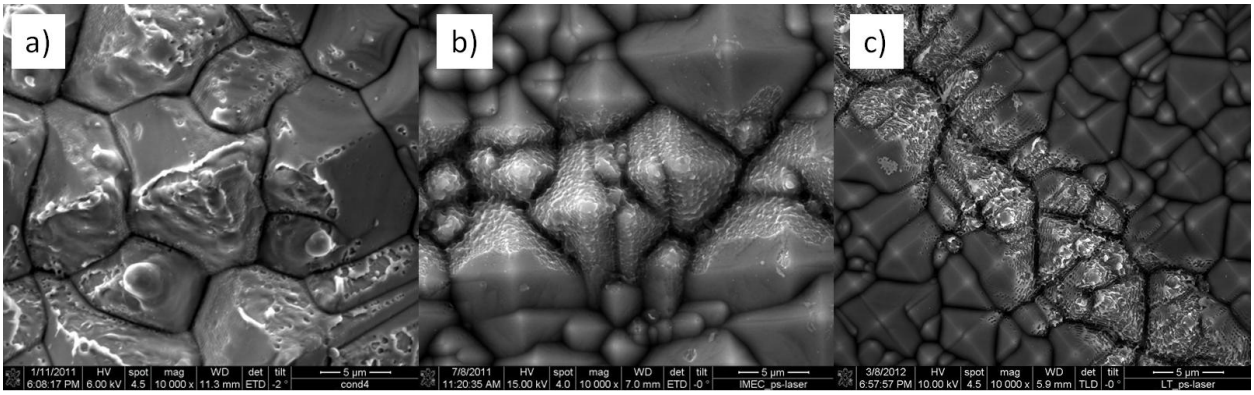


Figure 6.11. Scanning electron microscope (SEM) images on alkaline textured surfaces of (a) ns-UV laser ablation (5 µJ/pulse, 25% pulse overlap) of PECVD SiNx (85 nm), (b) ps-UV laser ablation (0.5 µJ/pulse, 50% overlap) of PECVD SiNx (85 nm), and (c) ps-UV laser ablation (0.5 µJ/pulse, 50% overlap) of SiO_2/SiN_x: 20/65 nm.

To characterize ps-UV ablation thresholds of different dielectrics, we followed the methodology described by Hermann et al. [HER10a]. Assuming a perfect Gaussian beam (quality factor M^2=1), the spatial fluence profile is given by:

$$\emptyset(x,y) = \emptyset_0 \cdot e^{-2\left(\frac{\sqrt{x^2+y^2}}{\omega_0}\right)^2} \tag{6.11}$$

where x, y are the distance from the beam center in both directions, ω_0 is the $1/e^2$ radius of the profile in the focal plane, and $\emptyset_0$ is the maximal laser fluence at the beam center (see Figure 6.12a). Using the relation between pulse energy E_p and fluence distribution:

$$E_p = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \emptyset(x,y)dxdy, \tag{6.12}$$

the maximum fluence can be defined as:

$$E_p = \frac{2\cdot\emptyset_0}{\pi\cdot\omega_0^2} \tag{6.13}$$

We then define the fluence $\emptyset_{thb}$ as being the threshold fluence at which the vapor pressure caused by melting of the underlying Si is sufficient to break and lift-off the dielectric layer(s) from the Si substrate and form an ablated spot of diameter D (see figure 6.12a). With this assumption and using equation (6.11), $\emptyset_{th\,b}$ can be related to D according to:

$$D^2 = 2\cdot\omega_0^2\cdot\ln\left(\frac{\emptyset_0}{\emptyset_{th\,b}}\right) \tag{6.14}$$

On the basis of equation (6.14), we can then determine the $1/e^2$ beam radius ω_0 and the melting threshold $\emptyset_{th\,b}$ experimentally for various dielectrics on alkaline textured surfaces.

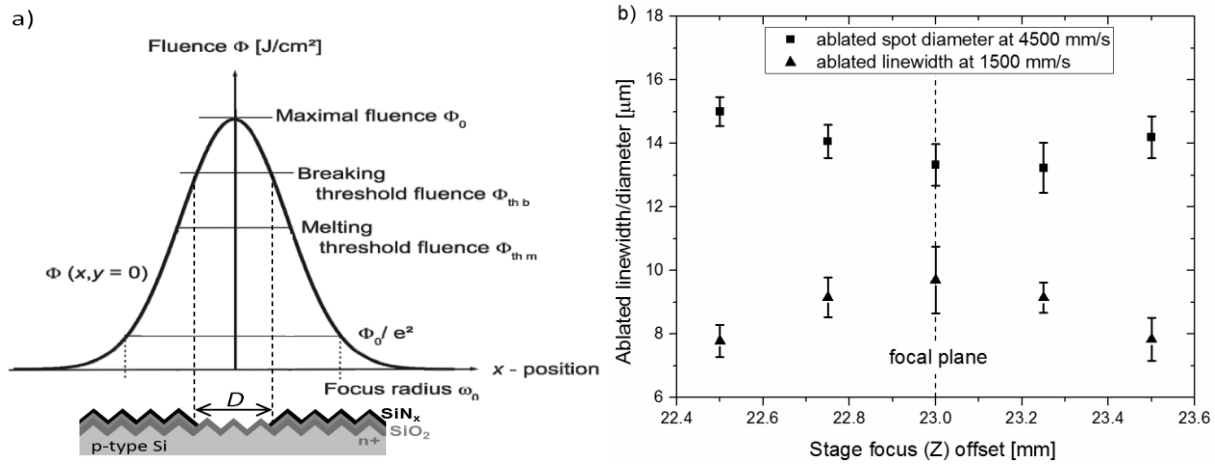


Figure 6.12. (a) Schematic of the spatial fluence profile of a Gaussian beam adapted from [HER10ba]. For a given focal beam radius ω_0 and a maximal energy fluence $\emptyset_0$, the molten laser spot diameter D correlates with the breaking threshold fluence $\emptyset_{th\,b}$ using equation (6). (b) Stage focus (Z-axis) optimization.

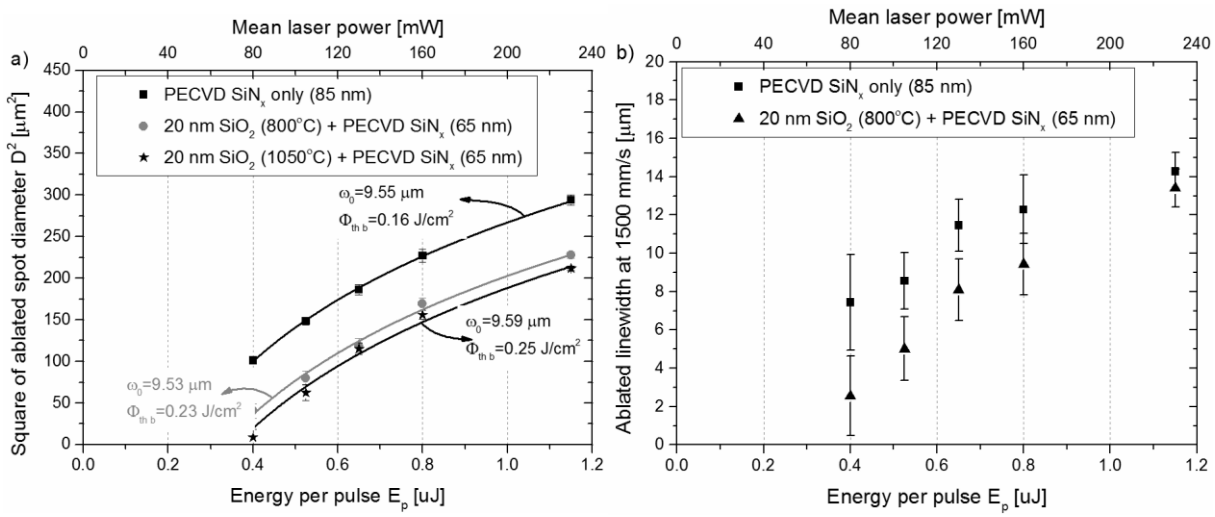


Figure 6.13. (a) Square of measured ps-UV laser ablated spot diameters D^2 versus applied pulse energy E_p for a single SiN_x ARC (■) and two different thermal oxide/SiN_x DARC (● and stars) on alkaline textured surfaces. Experimental data is fitted according to equations (6.13) and (6.144) with focus radius ω0 and threshold breaking fluence $\emptyset_{th\,b}$ as fit parameters (lines) and the obtained fit values are given in the graph. (b) Ablated line widths versus $E_p$at a scanning speed of 1500 mm/s for a single SiN_x ARC (■) and a thermal oxide/SiN_x DARC (▲). For all cases, thicknesses of dielectrics are measured on planar Si(100) undoped wafers (i.e. test wafers).

We fabricated i-PERC solar cells according to the sequence given in Figure 6.1 and we varied the front dielectric stack by doing thermal oxidation (i.e. emitter drive-in) either at 1050˚C or at 800˚C. In a third case, we also removed the front thermal oxide and adjusted the subsequent PECVD front SiN_x deposition time to obtain the same minimum reflectance at 620 nm. The stage focus offset was first adjusted to the wafer thickness, as shown in Figure, to obtain minimal line widths using a set of ps-UV ablation parameters (0.5 µJ/pulse, scanning speed=1500 mm/s).

We use scanning electron microscopy (SEM) images to measure the individual laser spot diameters (4500 mm/s scanning speed) and plot the square of spot diameters D^2 versus the corresponding pulse energy E_p. We determine the applied pulse energy by dividing the measured mean laser power (thermopile sensor) by the used repetition rate (200 KHz). Figure 6. shows the measured data for the three different front dielectric configurations. We fit the experimental data according to equation (6.14) using ω_0 and $\emptyset_{th\,b}$ as fit parameters and the obtained values are given in Figure 6.13a. As expected from the fact that we used the same ps-UV laser, the fit results show constant focus radii ω_0 for the different dielectric configurations. The breaking threshold fluence $\emptyset_{th\,b}$ are found to be higher in the case of thermal oxide/SiN_x DARC ($\emptyset_{th\,b}$~0.23-0.25 J/cm^2) than with a single SiN_x ARC ($\emptyset_{th\,b}$~0.16 J/cm^2). This explains the ablation results observed in Figure 6.11. As discussed in next section, ~10% more light is reflected at the wavelength used for ablation (λ=355 nm) for the present DARC (SiO_2/SiN_x: 20/65 nm) than for a single SiN_x ARC thereby explaining partly the increased breaking fluence threshold. The fact that thermal oxide is grown and not deposited as SiN_x might also play an important role. Breaking fluence thresholds obtained correspond fairly well with literature, such as ~0.2 J/cm^2 for ps-UV ablation of 110 nm thick thermal oxide on planar Si(100) [HER10b].

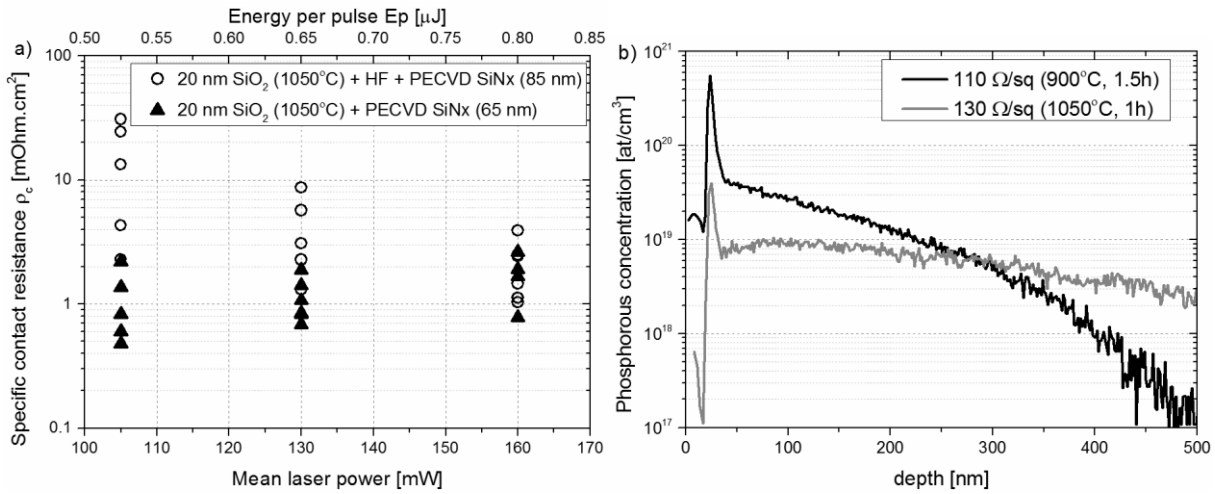


Figure 6.14. (a) Specific contact resistance ρ_c vs. mean laser power for cells with (▲) and without (○) thermal oxide (thicknesses of dielectrics are measured on planar Si(100) undoped). ρ_c values were measured after sintering for 4 min at 250˚C (b) Secondary-ion mass spectroscopy (SIMS) depth profile of phosphorous-doped emitters after oxidation at 1050˚C or at 900˚C. Thermal oxide is present at the surface.

Unsurprisingly, ablated line widths are found to be narrower at a given pulse energy for a thermal oxide/SiN_x DARC than for a single SiN_x ARC (see Figure 6.13b). Also the opened fraction might be lower which would affect specific contact resistance values (ρ_c) as we only consider the effect of line width in the calculations. To test this, we fabricated i-PERC solar cells according to the sequence given in Figure 6.1 (1 µm deep emitter, Ns~1x10^{19} cm^{-3}). For half of the cells the thermal oxide was removed in HF1% prior to front PECVD SiN_x. The scanning speed was adapted to keep a constant 50% pulse overlap as the mean laser power was increased. TLM test structures diced from finished cells were used to obtain ρ_c values after sintering for 4 min at 250˚C. Results are given in Figure 6.14a. Surprisingly, while relatively low ρ_c values ~0.5-3 mΩ.cm^2 are obtained for samples with thermal oxide independently of mean laser power, ρ_c values are found for samples without thermal oxide in the range of 2-30 mΩ.cm^2 at 105 mW and at 1-4 mΩ.cm^2 at 160 mW. Such differences at low mean laser power cannot be explained by differences in line widths because ρ_c values were extracted assuming identical line widths (8 µm for 105mW) for both type of samples while we know ablated line widths are slightly wider for samples without thermal oxide. In the present emitter two-step sequence, thermal oxidation is performed on a shallow emitter with high N_s. This leads to the incorporation of a high amounts of phosphorous (P) in the thermal oxide as shown from the SIMS profile given in Figure 6.14b. High P concentrations in the thermal oxide have previously been reported for low temperature oxidation (800˚C) of conventional 80 Ω/sq emitters and were confirmed by X-ray photoelectron spectroscopy (XPS) measurements [PRA12]. Though ps-UV ablation have been described to induce no emitter profile modifications due to the ultra-short interaction time with Si [KNO09a], it is speculated that at low mean laser power some P present in the thermal oxide is incorporated in Si. Future SIMS analysis after ps-UV ablation could confirm this. As the active surface concentration is relatively low (N_s~1x10^{19} cm^{-3} for 1050˚C oxidation), any slight increase in

active surface concentration coming from ps-UV ablation of P-containing thermal oxide might reduce ρ_c values obtained with Ni_2Si contacts. Possibly, this effect is much less pronounced for emitters with higher N_s. At high laser mean power, the contact area is more uniformly ablated (see Figure 6.16) thus ρ_c values are comparable independently of the presence of thermal oxide or not. It is also interesting to point out that the high incorporation of P in the thermal oxide might degrade both the thermal oxide optical and surface passivation properties and also affect its etch rate in HF, thus impacting parasitic plating. Again, it would be interesting for future investigations to change the emitter formation sequence so that thermal oxidation is performed once the surface concentration has been reduced (e.g. etched back emitters as in [LAC12] thereby limiting P incorporation as shown in [PRA12].

Optimization of ps-UV laser ablation parameters was then performed to minimize emitter bulk and surface damage while ensuring sufficient mechanical adhesion. Large area (12.5x12.5 cm^2) p-type, 1-2 Ω.cm, m-CZ-Si wafers were processed into i-PERC solar cells according to the sequence given in Figure 6.1 (1 µm deep emitter, Ns~$1x10^{19}$ cm^{-3}). Within each wafer, four mini-cells (25 cm^2, 2 busbars) were patterned by ps-UV laser ablation. Each mini-cell was patterned at a different mean laser power (80, 100, 130, and 160 mW) adapting the scanning speed for each condition to maintain a 50% overlap. Subsequently, the mini-cells were laser-cleaved (area=27 cm^2) and Ni/Cu/Ag plated. As the edge of the mini-cells was exposed to the plating electrolytes, the mini-cells had to be laser-cleaved again (area=26 cm^2) to remove the edge shunts. Finally, electrical parameters were measured before and after sintering at 250˚C for 4 min. As mentioned before, virtually all electrical parameters improved upon sintering indicating that no significant junction damage is occurring upon sintering. It appears that a mean laser power of 80mW in insufficient to fully open the front DARC as shown by series resistance values >0.5 Ω.cm^2 and consequently fill factors < 76% after sintering (see Figure 6.15). On the other hand, open-circuit voltage and pseudo-fill factor (pFF) values slightly degrade with increasing mean laser power indicating some degree of emitter surface and bulk damage caused by ps-UV laser ablation even though the junction is 1 µm deep. At optimum process conditions (mean laser power ~105-130 mW), average pFF values are on a much lower level (pFF~78-81%) level than with large area cells reported in this thesis (pFF>82%). This can be understood by the fact that mini-cell edges are left un-passivated by the laser-cleaving process resulting in increased ideality factors and hence lower pFF values. This effect is particularly important for small area cells as the perimeter to area ratio is larger and losses by up to 1-2%$_{abs.}$ were estimated by Abbott [ABB06] for edge-cleaving of 8 cm^2 p-type samples.

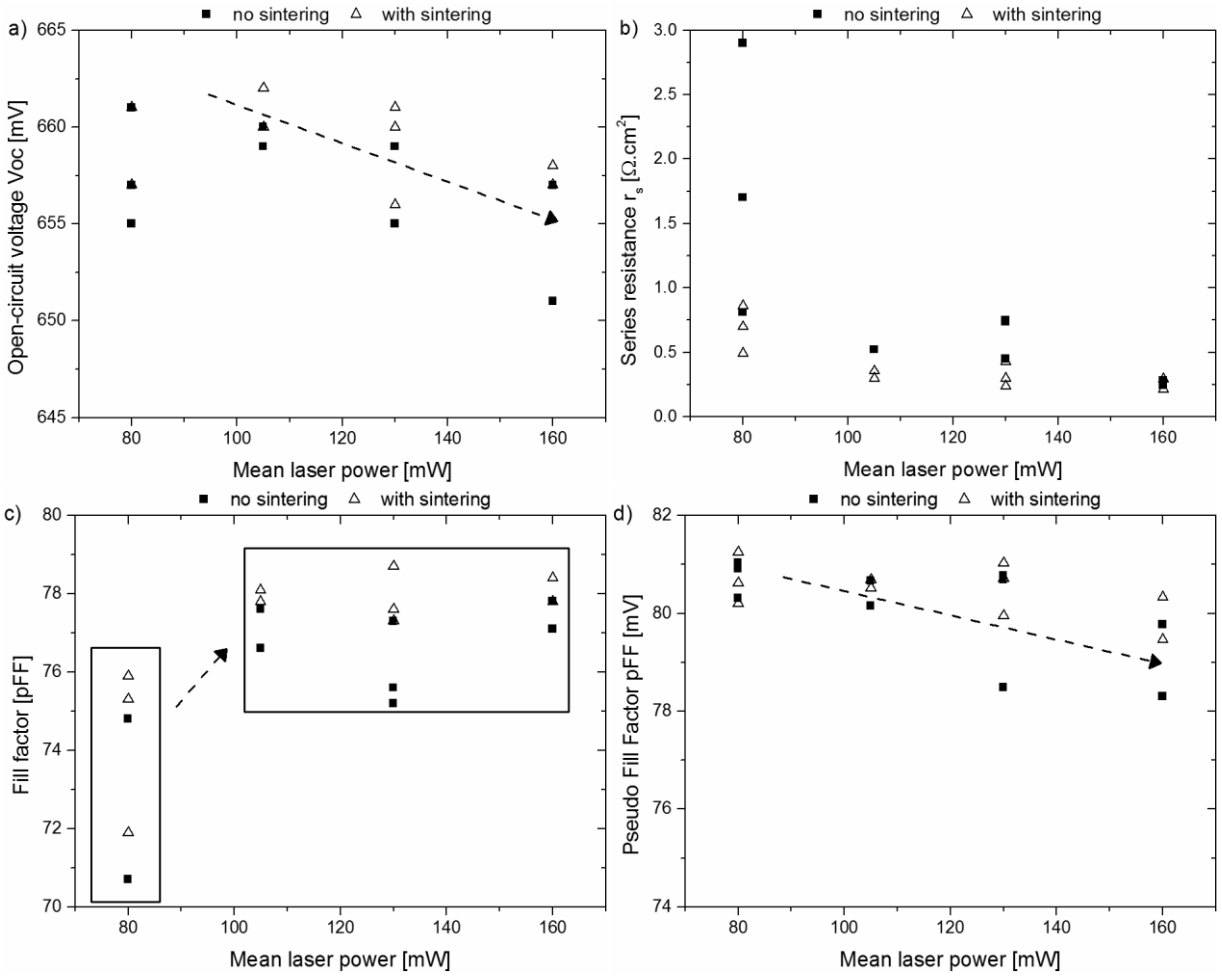


Figure 6.15. (a) Open-circuit voltage, (b) series resistance, (c) fill factor, and (d) pseudo fill factor of 25cm^2 i-PERC cells before (■) and after (Δ) sintering for 4min at 250˚C versus mean laser power. Pulse overlap is kept at 50%.

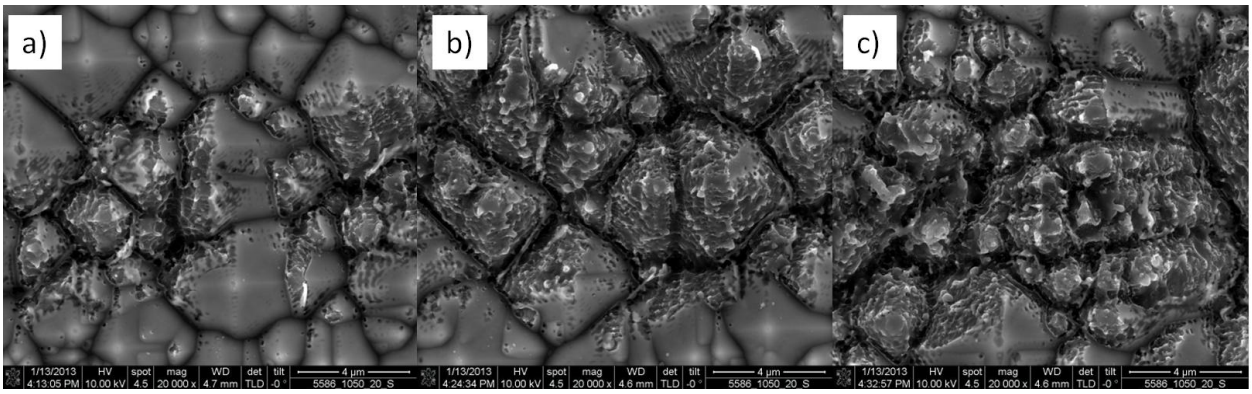


Figure 6.16. Scanning electron microscopy images of ps-UV ablated lines of thermal oxide/SiNx double-layer anti-reflective coating on alkaline textured wafers for various mean laser power conditions: (a) 80 mW, (b) 130 mW, and (c) 160 mW. Pulse overlap is kept at 50%.

Looking at SEM images of ablated lines at the various ps-UV laser conditions tested we can confirm that 80 mW mean laser power leads to finger discontinuities (see Figure 6.16a) as opposed to 130 mW (see Figure 6.16b). Possibly, such discontinuities at low power could be resolved by reducing the scanning speed to increase the pulse overlap beyond 50%. However, not only this would increase processing time but it would also lead to more areas receiving multiple times the fluence required for ablation (i.e. increase laser damage). Molten pyramid tips are visible at 160 mW (see Figure 6.16c) indicating extensive surface damage. Transmission electron microscopy images were taken at this high power in an attempt to visualize extended crystal defects that would extend deep into the junction and that could explain the measured pFF degradation. However, analysis performed were inconclusive possibly indicating that such defects are only present at limited locations. Defect etching investigations to reveal such locations prior to TEM are being started at imec and are the focus of another PhD thesis.

Tests were performed to evaluate the mechanical adhesion of the Ni/Cu/Ag plated mini-cells after sintering. Fingers adhesion was evaluated using a simple scotch tape peel test while adhesion in busbar areas was evaluated by recording the maximum solder tab adhesion at 45˚ pull angle. Both procedures are presented in details in Chapter 7. From the results given in Table 6.8, there is some evidence that 80 mW leads to worse finger adhesion as compared to other ps-UV laser ablation conditions. This is most likely caused by the finger discontinuities seen in SEM images. Pull tab adhesion results are relatively comparable for all groups (average ~2 N/mm) except at 130 mW due to some outliers points giving zero adhesion.

Table 6.8: Finger peel test (scotch tape) and solder tab adhesion results of 25 cm^2 i-PERC cells for various mean ps-UV laser powers. Procedures to evaluate mechanical adhesion are presented in details in Chapter 7.

Mean laser power [mW]	Finger peel test (maximum # fingers=18)				Maximum pull tab adhesion at 45deg (N/mm)				Average adhesion (N/mm)
80	0	18	0	18	0	2.68	2.53	3.58	
80	18	18	0	0	1.94	2.02	1.47	0.87	2.06
80	1	9	0	0	5.29	1.87	1.77	0.68	
105	0	0	0	0	1.98	0.78	1.3	1.92	
105	0	0	0	18	2.82	2.44	4.96	1.65	2.12
105	0	0	0	0	1.85	1.98	1.33	2.56	
130	0	0	0	0	2.52	0.93	0	0	
130	0	9	0	1	2.27	0.84	2.54	2.85	1.48
130	0	0	0	0	2.59	3.25	0	0	
160	0	0	0	0	0.61	0.67	2.36	2.71	
160	0	0	0	0	1.77	3.28	1.64	3.19	2.19
160	0	0	0	0	3.82	1.19	3.71	1.27	

6.2.4. Front dielectric(s)

Native oxide is known to inhibit nickel silicide formation and hence a native oxide removal step is required prior to nickel deposition (see Chapter 5.2). Native oxide removal using diluted hydrofluoric acid (HF-dip) was already present in the original LGBC cell process patented by Green and Wenham in 1984 (see Chapter 3.2.6) and hence it is no surprise that we also implemented an HF-dip prior to Ni plating. To demonstrate the need for sufficient HF-dip prior to Ni plating, we prepared small-area (5x5 cm^2) i-PERC solar cells using the simplified Ni/Cu/Ag plating sequence given in Figure 6.1 and optimized ps-UV laser ablation parameters (see previous section). From the results given in Table 6.9, not only insufficient pre-cleaning (HF1%, 1min) leads to higher series resistance (r_s) after sintering (r_s=0.86 $\Omega.cm^2$ as opposed to r_s=0.81 $\Omega.cm^2$ with HF2%, 2 min) but it also gives worse diode characteristics. The worse diode characteristics (increased ideality factors at 0.1sun thus reduced pseudo-fill factors) can be explained by the presence of localized Schottky contacts. Optimum pre-cleaning conditions will depend on the emitter profile, dielectric layer(s) and patterning technique used.

Table 6.9: Average (over 3 cells) electrical parameters for small area (5x5 cm^2) i-PERC solar cells featuring a 1 µm deep emitter and Ni/Cu/Ag contacts sintered for 4min at 250˚C for various pre-clean conditions in diluted HF. HF1% is prepared by mixing 2 parts of HF49% with 98 parts of de-ionized water.

Devices	pFF (%)	r_s ($\Omega.cm^2$)	n at 1sun	n at 0.1sun
HF1%, 1 min before sintering	82.3	0.863	1.13	1.13
HF2%, 2 min before sintering	82.4	0.892	1.15	1.11
HF1%, 1min after sintering	79.1	0.858	1.11	2.23
HF2%, 2min after sintering	82.4	0.814	1.07	1.18

The need for a HF-dip prior to Ni/Cu/Ag plating poses additional requirements for the front dielectric(s). Not only the front dielectric(s) should limit optical and recombination losses but their property as plating mask (i.e. Ni/Cu/Ag plating only in the finger and busbar areas) should not be degraded by the HF-dip step. To meet this third requirement, the original LGBC process relied on a thick thermal oxide while the LGBC process commercialized by BP Solar relied on LPCVD Si_3N_4 (see Chapter 3.2.6) as both layers are dense and virtually pinhole free. However, thick thermal oxide is not optimum to limit front reflectance losses and, unlike PECVD SiN_x, both layers do not give sufficient bulk passivation via hydrogen release [RIC04]. PECVD SiN_x would be more ideal as front dielectric but it is typically less dense (due to lower deposition temperature [CLA85]), less “particle-free”, and contains pinholes, all of which lead to the phenomenon referred to as “ghost plating”, “parasitic plating”, or “over plating” [WAN09, BRA11b]. Optimization of front dielectric(s) making use of PECVD SiN_x requires to know what parameters are affecting parasitic plating and what can be done to minimize it.

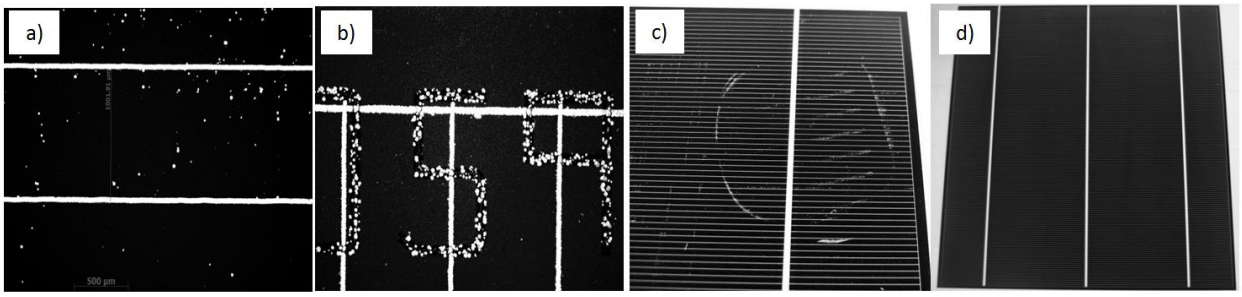


Figure 6.17. (a) Parasitic plating in single PECVD SiNx layer, (b) parasitic plating in SiO_2/SiN_x double layer anti-reflecting coating (DARC) caused by non-conformal SiNx deposition along laser scribed areas, (c) parasitic plating in SiO_2/SiN_x DARC caused by mechanical stress (vacuum wand), (d) cell processed at optimum conditions.

Impurities/particles present at the surface prior to PECVD SiN_x, cracks due to mechanical stress, non-conformal SiN_x deposition along sharp angles, and high pinholes densities, all which cause unwanted openings in SiN_x are believed to be the main causes for parasitic plating [WAN09, BRA11b, LEE11, KYE12]. Similar observations were made during this thesis such as: pinholes in PECVD SiN_x (Figure 6.17a), laser-marking prior to alkaline texturing causing non-conformal SiN_x deposition (Figure 6.17b), and vacuum wand causing mechanical stress (Figure 6.17c). Insufficient saw damage removal on diamond-sawn wafers (deeper crystal damage than standard wire-sawn wafers) was also found to lead to substantial parasitic plating. In our experience, implementing a SiO_2/SiN_x double-layer anti-reflective coating (DARC), using a higher PECVD deposition temperature to make the film denser, and using handling procedures to limit scratching were the most significant steps to circumvent parasitic plating as shown in Figure 6.17d. On top of these solutions, others have listed: implementing cleaning procedures to remove residues prior to PECVD [BRA11b, KYE12], optimizing the SiO_x-SiN_x selectivity by using buffered HF [LI11, KYE12], adapting PECVD SiN_x deposition parameters (pressure, gas flows, stoichiometry, etc.) to get denser and more conformal layers [WAN09, LEE11], or rounding the acidic texture on multi-Si [WAN09].

In the particular case of SiO_2/SiN_x DARC, the thickness of the thermal oxide needs to be carefully optimized as to circumvent parasitic plating without increasing dramatically optical losses. Additional limitations might appear for multi-Si such as bulk lifetime degradation due to high temperature processing (also present with standard CZ-Si as discussed in the previous section) or insufficient bulk hydrogenation for thick SiO_2 layers [TJA08]. The free freeware optical calculator named OPAL 2 and its built-in complex refractive index library [MCI12] were used to simulate the impact of various thermal oxide thicknesses on the front optical losses. Simulations were performed using the complex refractive index values from Palik [PAL85] for thermal oxide and from Duttagupta et al . [DUT12] for PECVD SiN_x (n=2.03) as they were the closest to values measured for our layers. A characteristic base angle of the pyramid structures of 54.74˚, a substrate thickness of 160 µm, and a number of light passes Z of 25 were taken as being representative of our standard i-PERC devices (see section 6.1). The SiN_x thickness was re-optimized for each thermal oxide thickness to give the minimal reflectance loss.

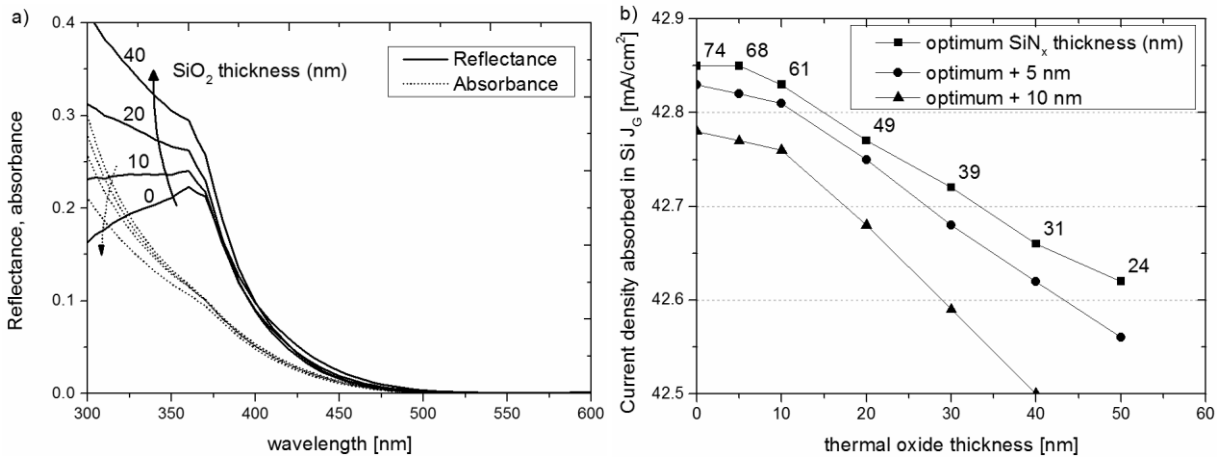


Figure 6.18. (a) Simulated reflectance and absorbance vs. wavelengths curves for various SiO_2 thicknesses. For each thickness the front SiN_x thickness was optimized. (b) Simulated current densities absorbed in Si for various SiO_2 thicknesses, for each thickness the optimum SiN_x thickness is given. All simulations were performed using the freeware OPAL2 [MCI12]. Parameters used for simulations are given in the text.

Increased SiO_2 thicknesses are found to lead to higher reflectance losses at very short wavelengths (<400 nm) as shown in Figure 6.18a. Using the latest version of the AM1.5g spectrum as incident spectrum, we find for SiO_2<10 nm that optical losses are practically negligible as compared to SiN_x only (see in Figure 6.18b) while for SiO_2>10 nm they account for a loss of about 0.1 mA/cm^2 in short-circuit current density (j_{sc}) per 20 nm extra of SiO_2. Adding typical wafer-to-wafer variations in nitride thickness of 5 nm, we could expect j_{sc} losses by up to 0.15 mA/cm^2 for a thermal oxide thickness of 30 nm at the front side as compared to SiN_x only. Conversely, reducing the front thermal oxide thickness by 10 nm, we estimate a gain in j_{sc} by up to 0.1 mA/cm^2. Large area (12.5x12.5 cm^2) i-PERC solar cells were processed according to the sequence described in Figure 6.1. For one group, the oxide thickness was reduced to 10 nm (measured on Si(100) undoped) by adjusting the oxidation time and the front PECVD SiN_x thickness was adjusted accordingly. No other parameters was changed and consequently the emitter sheet resistance (R_{sh}) values were slightly lower for the group with only 10 nm SiO_2. Instead of the expected 0.1mA/cm^2 gain in j_{sc} for this group, we observed a 0.1 mA/cm^2 drop as shown in Table 6.10. This result can be explained by the fact that the front SiO_2 is now too thin to withstand the HF-dip and consequently parasitic plating is present on these cells leading to shading losses. The presence of parasitic plating is reflected in the increased busbar-to-busbar resistance R_{bb} (i.e. finger resistance) values since plating occurs partially at the SiN_x pinholes instead of only at the front metal grid. This is turns affects the series resistance and consequently the fill factor of these cells. In addition, open-circuit voltage (V_{oc}) values are found 5 mV lower. Based on emitter dark saturation current densities V_{oc} losses can be attributed to increased Auger recombination losses in the emitter due to the lower R_{sh} values. These results demonstrate that circumventing parasitic plating is more important than reducing the front SiO_2 thickness by 10 nm to potentially gain 0.1 mA/cm^2.

Table 6.10: Average (over 4 cells) electrical parameters for large area (12.5x12.5 cm^2) i-PERC solar cells processed according to Figure 6.1. For one group, the thermal oxide thickness (measured on planar Si(100) undoped) was reduced to 10 nm by adjusting the oxidation time (emitter drive-in time under N_2 is kept identical).

Thermal oxide thickness		j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	η [%]	r_s [$\Omega.cm^2$]	n	pFF [%]	R_{bb} [mΩ]
20 nm	Avg.	38.8	660.0	77.8	19.9	0.87	1.12	82.4	28.2
	stdev	0.1	2.0	0.6	0.1	0.17	0.02	0.2	1.1
10 nm	Avg.	38.7	655.0	77.0	19.5	0.90	1.17	81.8	34.6
	stdev	0.1	2.0	0.8	0.3	0.08	0.04	0.5	8.5

6.2.5. Front metal grid

Simulations performed at the beginning of this chapter suggested that higher efficiencies could be achieved by optimizing the front metal grid design. Optimization of the front grid design was performed to some extent when transferring the simplified plating sequence on 15.6x15.6 cm^2 substrates to the MECO plating and BTU sintering tool and we could demonstrate short-circuit densities close to 39 mA/cm^2 together with fill-factors close to 80% leading to efficiencies up to 20.8% (see Chapter 5.4.5). Complete front metal grid optimization for a specific emitter profile requires to adjust both the finger pitch and the plating thickness simultaneously. This requires a large number of wafers and hence optimization of the front metal grid was performed during this thesis by adjusting the finger pitch and the plating thickness separately. An example of plating thickness optimization is presented in this section and results are compared to simulated results obtained from grid modeling as described in Chapter 4.

Large area (12.5x12.5 cm^2) p-type, 1-2 Ω.cm, m-CZ-Si wafers were processed into i-PERC solar cells featuring a 140 Ω/sq 1 μm deep emitter. Contact openings were defined using ps-UV laser ablation and nickel silicide formation (300˚C, 30s) was performed directly after sputtering of thin Ni layer (40 nm). Unreacted Ni was removed in diluted H_2O_2:H_2SO_4 (1:8) in 30s, the surface was re-activated by dipping the samples in HF1% for 1 min, and the contacts were thickened by bias-assisted LIP Ni (~1 μm) prior to electroplating of Cu. No Ag capping was applied. Illuminated I-V measurements were performed after plating an initial thickness 4 μm of Cu and re-measured each time after plating an additional couple of μm of Cu. Since the XRF thickness measurement tool (see appendix B) was not yet available at imec, plated thickness were estimated from Faraday's Law (see equation (2.13) in Chapter 2) assuming an electrolyte efficiency of 100% and a density of 8.94 g/cm^3 for Cu). For the grid design simulations the "standard" values given in Table 4.3 in Chapter 4 were used except for a few parameters that are given in Table 6.10. Namely these "non-standard" parameters account for: (i) the different substrate size and resistivity that were used, (ii) a measured lower bulk lifetime and higher rear surface recombination velocity leading to a higher j_{0b}, (iii) a measured sheet resistance of ~140 Ω/sq, and (iv) a measured specific contact resistance of ~1 $m\Omega.cm^2$.

Table 6.10: Parameters specifically used for the simulations given in Figure 6.20. Other "standard" parameters are given in Table 4.3 in Chapter 4.

Assumed parameters		
Symbol	Definition	Used value
A_{cell}	Cell area	125x125mm^2
j_{0b}	Base and rear side dark saturation current density	198.4 fA/cm^2
j_{02}	Dark saturation current density (n=2)	7x10^{-9} A/cm^2
R_{sh}	Sheet resistance of the emitter	140 Ω/sq
ρ_{bus}, ρ_f	Resistivity of Cu plated busbars and fingers	2.0x10^{-6} Ω.cm at 25˚C
ρ_b	Bulk resistivity	2 Ω.cm
ρ_c	Specific contact resistance of Ni	1 mΩ.cm^2

Measured illuminated I-V results are given in Figure 6.20 together with simulated results as a function of Cu plating thickness. A relative good agreement in found between measured and simulated fill-factors (FF), short-circuit densities (j_{sc}), busbar-to-busbar resistances (R_{bb}), open-circuit voltages (V_{oc}), and efficiencies. One could argue that this is simply the result of the large number of fit parameters. Nevertheless, this demonstrates that such grid modeling simulations can be useful to optimize the front grid design as described in Chapter 4. Unsurprisingly, j_{sc} values decrease linearly with plated thickness while FF and R_{bb} quickly saturate with increased thicknesses (see Figure 6.20a). This illustrates the challenge of obtaining high FF and j_{sc} values simultaneously. For R_{bb}, it is interesting to point out that a resistivity ρ=2 μΩ.cm for Cu was required to fit the data. The difference with pure Cu (ρ_{Cu}=1.7 μΩ.cm) is most likely coming from the fact that in this experiment plated Cu was not annealed since we reported a drop of 10-15% in resistivity upon annealing (see Chapter 5.4.3). Overall, we find an optimum plating thickness in the range of 7-12 μm for these cells (see Figure 6.20b). The broad optimum can simply be explained by the fact that, in this range, j_{sc} losses with increasing Cu thickness are compensated by higher FF values.

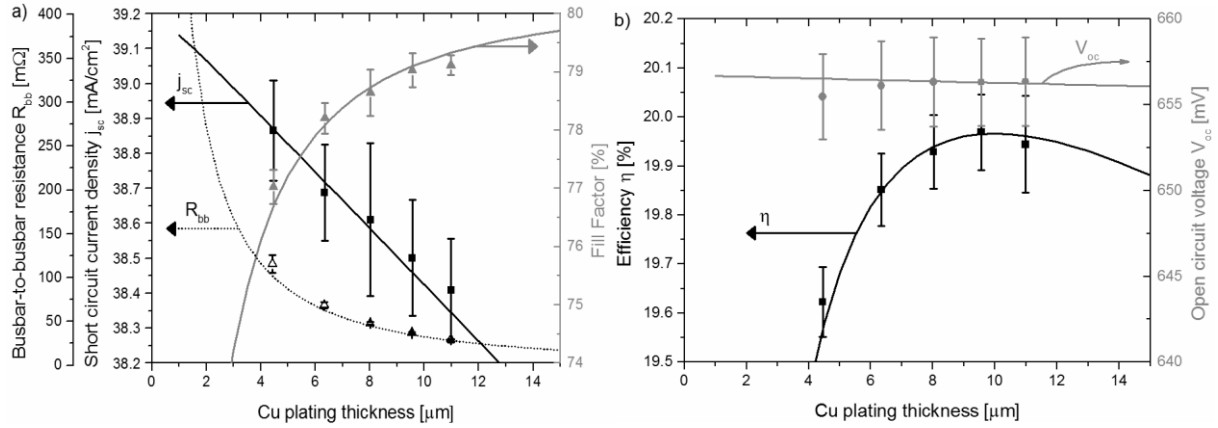


Figure 6.20. (a) Measured (symbols) and simulated (lines) short-circuit current density (■), fill factor (▲), and busbar-to-busbar resistance values vs. Cu plating thickness. (b) Measured (symbols) and simulated (lines) open-circuit voltage and efficiency values vs. Cu plating thickness. Measured data (averaged over 5 wafers) was obtained on large area (12.5x12.5 cm^2) i-PERC devices featuring a 1 μm deep 140Ω/sq emitter and Ni/Cu/Ag plated contacts.

6.2.6. Internal rear reflectance

Simulations performed at the beginning of this chapter suggested that improving the internal rear reflectance from 95% for our current best i-PERC devices to 98% would lead to 0.3%$_{abs.}$ gain in efficiency. To improve the internal rear reflectance it is necessary to understand the formation of local Al-back surface field (BSF) contacts in i-PERC devices and its impact on internal rear reflectance. These aspects are shortly discussed in this section.

The formation mechanisms of the local Al-BSF in i-PERC devices are well described in literature [URR10, MULL12, URU12a]. In this thesis, local Al-BSF formation is achieved by firing i-PERC devices with a thin sputtered (PVD) Al layer in a belt furnace (few seconds at ~800˚C peak wafer temperature). Laser ablation of the front dielectric(s) and front Ni/Cu/Ag plating are applied after firing. During firing, solid Si in contact with Al (at the laser opened areas) dissolves in liquid Al at high temperature. After reaching the peak firing temperature, the wafer cools down and Si atoms diffuse back to the contact areas where they re-grow epitaxially leading to Al incorporation in the Si lattice (Al-p^+). The local Al-p^+ leads to a high-low junction within the p-type Si base acting as a back surface field (BSF) effectively passivating the contacts. The Al-p+ thickness that is controlling the contact recombination has been shown to be strongly influenced by the size and spacing of the contacts (L_p), the Si content in Al, the boron content in Al, the firing temperature, as well as the opening technique of the dielectric layer [URR10,MULL12, RAU12]. In the particular case of laser ablation and thin sputtered Al layer, local Al-BSF formation results in inverted pyramid contacts as shown in Figure 6.21a. After contact firing, several individual mechanisms, all of which occurred during contact firing, can lead to a drop in internal rear reflectance compared to the situation before firing:

- large imprint size with high parasitic absorption blocking subsequent light bounces
- free carrier absorption (FCA) in the BSF (not discussed here)
- degradation of Al reflectance by incorporation of Si through the alloying process
- degradation of dielectric reflectance by reaction with Al or Si present in Al (Figure 6.21b)
- reduced Al coverage due out-gassing of hydrogen contained in rear dielectrics

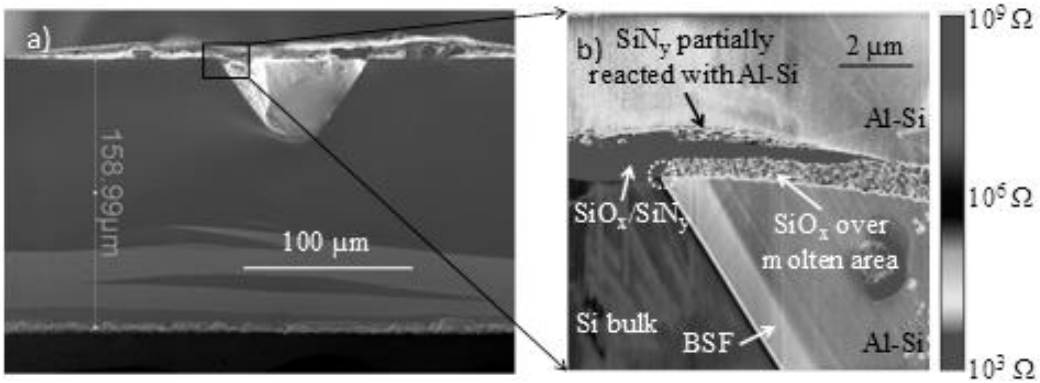


Figure 6.21 (a) Scanning electron microscope (SEM) picture of local Al-BSF contacts. (b) Spreading scanning resistance microscopy (SSRM) picture of the region located by a square in (a). Pictures are taken from [URU13b].

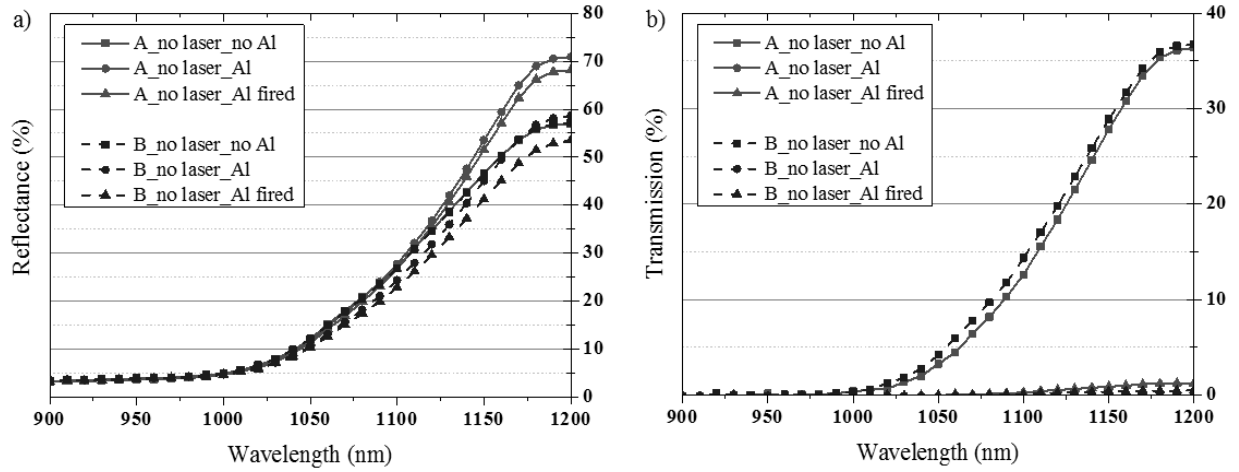


Figure 6.22 (a) Average, over 4 samples, reflectance (a) and transmission (b) measurements for stack A= $SiO_2/SiO_y/SiN_x/Al$ and stack B= $SiO_2/SiN_x/Al$. Error bars are not shown for clarity.

Test wafers were prepared for two separate experiments. No $POCl_3$ diffusion was done to prevent FCA in the emitter to affect reflectance measurements in the 900-1200 nm range.

In a first experiment, the rear dielectric stack was varied (A = $SiO_2/SiO_y/SiN_x/Al$: ~20/400/120/2000 nm, B = $SiO_2/SiN_x/Al$: ~20/120/2000 nm) while keeping the front ARC identical (SiO_2/SiN_x). SiO_2 refers to a thin dry thermal oxide, while SiO_y/SiN_x refers to PECVD oxide/nitride respectively. No contact holes were present at the rear side. Reflectance and transmission measurements were done prior to PVD Al, after PVD Al, and after Al firing (~800˚C peak wafer temperature). Reflectance and transmission results are plotted in Figure 6.22a and in Figure 6.22b respectively. When no contact holes are present, firing pure Al only results in a ~2% drop in reflectance at 1200 nm which corresponds to light being transmitted through the wafer. Additional measurements (not shown here) confirmed that light transmission occurs at locations where Al is no more present on top of the dielectrics. This is likely caused by hydrogen out-gassing from SiN_x and displacing molten Al prior to wafer cool down. If a simplified stack B is used, the reflectance is at the same level prior to PVD Al than with the more complex stack A. After Al PVD and also after firing, stack B clearly shows a lower reflectance at 1200 nm than stack A. Since transmission losses did not increase significantly with stack B, light must be absorbed at the SiN_x/Al interface. The presence of a thick SiO_y in stack A forces light to arrive under different angles at the SiN_x/Al interface so that it is better reflected back into Si. Finally, it should be mentioned that replacing SiN_x by SiO_y in stack B resulted in even worse degradation of the rear reflectance after firing due to Al consuming SiO_y during firing.

The rear stack A was chosen for a second experiment. Wafers were divided into 4 zones: (i) no rear ablation, (ii) ps-UV ablation with an opening diameter of 20 µm and a dot pitch L_p = 600 µm, (iii) ns-UV ablation with an opening diameter of 40 µm and L_p = 600 µm (ns-laser), (iv) ns-UV ablation with an opening diameter of 50 µm and L_p = 600 µm (ns-laser #2). Al PVD or $AlSi_{12.7\%}$ PVD were deposited (~2 µm) and reflectance measurements were performed before and after firing. Figure 6.23 collects these results, in (a) with pure Al and in (b) with $AlSi_{12.7\%}$. It is found with $AlSi_{12.7\%}$ that the reflectance drops significantly after firing even without laser

openings, contrary to firing of pure Al, and that no further drop is observed if local Al-BSF contacts are formed. This demonstrates that Si present in $AlSi_{12.7\%}$ is the main cause for the rear reflectance loss upon firing (~20% loss at 1200 nm). The presence of Si in Al at the interface with SiN_x was confirmed by transmission electron microscopy (TEM) images and results are further discussed in [URU13b]. In the case of pure Al layers, the reflectance loss is caused by the amount of Si coming from the wafer via the laser openings during firing. Therefore, in order to minimize the internal rear reflectance loss upon firing it is critical to limit diffusion of Si into Al.

Several parameters have been shown to affect the diffusion of Si into Al. Incorporating Si into Al effectively reduces the diffusion of Si coming from the contact holes in Al [RAU11, URU12b]. However, this does not solve the internal rear reflectance problem as shown in Figure 6.22b. Reducing the opening diameter reduces Si uptake and hence reflectance losses (ps-laser vs. ns-laser, see Figure 6.23a). However, this was found to lead to increased series resistance losses [URU13b]. Reducing the firing peak temperature was also found to limit Si uptake [URR10, LAU11b]. However, this might also lead to thinner Al-p^+ [reference] and hence increased recombination at the contacts. Using thick Al pastes (typically ~20 µm) instead of thin PVD Al layers (~2 µm) increases the volume of Al available to dissolve Si and hence possibly limits lateral transport of Si thereby leading to reduced reflectance losses as reported by Cacciato et al. [CAC13]. Unsurprisingly, the use of alternative cell structures such as PERL or LFC (see Chapter 2.3.2) where high temperature is avoided appears to be the best solution. Using such cell structures in combination with Ni/Cu/Ag plated contacts, excellent internal rear reflectance results have already been demonstrated by other research groups [WAN09, LI13]. Investigations are currently being started at imec with some encouraging results in combination with Ni/Cu/Ag plated contacts being published for rear local p^+ obtained by selective epitaxy [REC13] or by laser doping [COR13]. In addition, such schemes present the advantage that the rear dielectric stack can be considerably simplified and optimized for its passivation and optical properties only [DAV13].

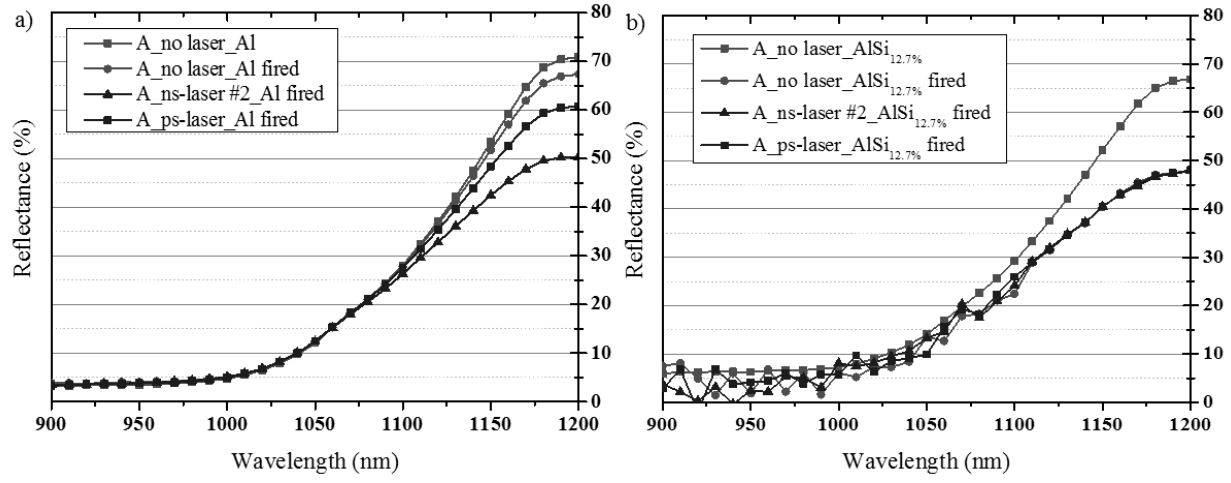


Figure 6.23 Average reflectance measurements with 2 µm PVD pure Al (a) and with 2 µm PVD AlSi12.7% (b).

6.3. Chapter summary

In the first part of this chapter, a simple analytical power-loss analysis of the best 12.5x12.5 cm^2 p-type i-PERC device (ŋ=20.5%) fabricated during this thesis was presented in an attempt to direct future efficiency improvements. The largest power losses in this device were found to be caused by recombination losses at $V_{oc,}$ followed by optical losses (mainly due to front grid shading losses), and by recombination losses due to non-ideal n factor. Efficiencies up to 20.8% were estimated from simple PC1D simulations when reducing front grid shading losses and were confirmed when transferring the simplified Ni/Cu/Ag plating sequence to 15.6x15.6 cm^2 substrates (see Chapter 5.4.3). Additional areas of improvements (rear dielectric passivation, rear internal reflectance, recombination under the front contacts) enabling efficiencies beyond 21.1% were identified and investigations are being started at imec in these directions. The fact that Schott Solar could recently demonstrate efficiencies up to 21.3% on large area (15.6x15.6 cm^2) [MET13] clearly supports our estimations that efficiencies beyond 21.5% are feasible on large p-type CZ-Si devices using Ni/Cu/Ag plated contacts.

In the second part of this chapter, the re-optimization of several p-type PERC processes required when implementing a simplified Ni/Cu/Ag plating sequence was presented together with in-depth analysis performed during the course of this thesis. Optimizing the front homogeneous emitter profile in a two-step approach ($POCl_3$ diffusion + thermal oxidation) we could demonstrate equivalent results (both electrical and adhesion results) when implementing a 0.5 µm deep emitter as compared to a high-efficiency 1 µm deep emitter. The use of a shallower 0.3 µm deep emitter was shown to be mainly limited by emitter surface and bulk damage caused during ps-UV ablation of the front dielectric(s) and not by diffusion of Ni and/or Cu during sintering. Thermal oxidation was shown to have significant impact on the bulk CZ-Si properties (e.g. metallic impurities decorating oxygen precipitates). The presence of a thin thermal oxide in a double ARC configuration (SiO_2/SiN_x stack) was found to: (i) increase the fluence threshold for front ps-UV ablation, (ii) increase front reflectance losses, and (iii) reduce parasitic plating. For all these cases, solutions were described and future areas of improvements were identified. An example of front grid design optimization (i.e. plating thickness optimization) was given validating part of the front grid modeling work described in Chapter 4. Finally, the mechanisms explaining internal rear reflectance losses in i-PERC devices upon firing were identified (mainly absorption at SiN_x/Al interface due to the presence of Si) and possible solutions to minimize or even eliminate this problem were briefly discussed.

From the results presented in this Chapter, it becomes clear that optimizing p-type PERC devices for Ni/Cu/Ag plated contacts requires to look at many different process steps since they are inter-related. Finally, to demonstrate industrial viability of these Ni/Cu/Ag plated contacts we should also address long-term reliability and cost-of-ownership. These aspects are discussed in Chapter 7 and in Chapter 10 respectively.

CHAPTER 7

Reliability of Cu contacts

The generally observed poor mechanical stability of Ni/Cu plated contacts as compared to screen printed Ag contacts is a great source of concern for industry thus it is addressed first in this chapter. As it was not obvious to us nor others [JON05, GAB06] that high pull force values were better for module reliability we also performed extended thermal cycling and damp heat testing and results are presented in section 7.3. We also looked at long-term reliability issues associated with the potential risks of Cu or Ni diffusion and results are presented in section 7.4.

7.1. Introduction

In Chapter 5 we developed a simple process sequence to define Ni/Cu/Ag plated contacts that uses industrial pilot-line tools and we could demonstrate solar cell efficiencies up to 20.7% on 15.6x15.6cm^2 substrates. However, it is not cell efficiencies that will trigger a major switch to copper metallization but rather the demonstration of a clear reduction in the levelized cost of electricity (LCOE) generation as compared with other metallization technologies. As the LCOE in $/kWh of a PV system requires considering its total cost and the energy generated over its lifetime [BRA11] it is crucial to ensure a reliable performance of the PV system. PV modules manufacturers typically market their product with a 20+ year warranty. Testing procedures such as IEC61215 or "VDE Quality Tested" (see Table 7.1) address the design qualification (safety, performance, etc.) of a PV module and were designed to weed out modules that would fair early in the field. However, they do imply long-term reliability in the field. An example of this is the fact that PV modules that had been certified according to IEC standards were failing in many existing PV installations due to a phenomenon called potential-induced-degradation (PID) [NAU13]. The lack of reliability standards is partially due to the fact that most modules in the field were only recently installed and also because module manufacturers or utilities owning PV power-plants are often not willing to share their data. IEC or VDE certifications should only be regarded as a minimum requirement until a PV module reliability standard is defined. Typically the most stringent IEC61215 tests are the environmental tests which consists in temperature cycles from -40˚C to +85˚C (TC), damp heat (DH) testing, and humidity-freeze (HF).

Table 7.1: Example of test matrix for IEC61215 and VDE Quality Tested. Adapted from [NEL13].

Required tests	IEC61215	VDE Quality Tested
Test frequency	Once, for initial certification	Continuous sampling, quarterly monitoring
Thermal cycling (TC)	200 cycles	400 cycles
Damp heat (DH)	1000 hrs.	1500 hrs.
Humidity freeze (HF)	10 cycles after 50 TC	10 cycles after 50 TC
Mechanical load test	Static test after DH	Dynamic load test before HF and TC

7.2. Adhesion

7.2.1. Introduction

Solar cells are typically interconnected in series by means of tinned Cu ribbons, or tabs, which are continuously (or in spots) soldered onto front busbars of the cell and from then onto rear busbar pads of the adjacent cell. Below the melting point of the solder, the different coefficients of thermal expansion (CTE) of Si, metal contacts, and Cu ribbons combined with thermal gradients can induce a high amount of stress. This stress can lead to the formation of microcracks in Si and/or the propagation of existing microcracks. Microcracks can result in parts of the cells being isolated thus reducing power output due to lower cell short-circuit current or higher series resistance. The resulting current mismatch in the string might cause the cell to operate in reserve bias thus increasing risks of failure due to hot spots (current flowing in small locations leading to a strong temperature increase thus damaging irremediably the module).

The soldering materials, process, and equipment as well as upstream cell processing and module manufacturing can influence stress in the modules. In case of a cell spot soldered, the shear stress (τ) induced by a ribbon is given by [WEN09]:

$$\tau = \int_0^l \frac{F}{A} \cdot dl = \frac{E \cdot S_0 \cdot c \cdot \Delta T \cdot \ln(l_k)}{b_k} \quad (7.1)$$

where E is the Young's modulus, S_0 the initial cross-sections, c the coefficient of thermal expansion (CTE), ΔT the temperature change, and the terms l_k and b_k stand for the length and the width of the contacted areas respectively.

Equation (7.1) shows that the most important parameters in order to minimize shear stress are the CTE, the Young's modulus, and the soldering temperature. Reducing the ribbon dimensions (S_0) would also be beneficial but, as discussed in Chapter 4, a balance needs to be found between resistive and shading losses at module level. The effect of ribbons parameters are discussed in literature [GAB06, WEN09, ZEM10]. Soft ribbons with a low Young's modulus and low yield strength are generally preferred as they induce less stress. On the other hand the advantage of low CTE ribbons is often negated by the fact that they are more resistive thus need to be thicker and also present a high yield strength. As they enable lower soldering temperature, Pb containing solders are preferred over Pb-free solders. Efforts have also been made in introducing tabbing equipment enabling spot soldering and with long cooling zones to minimize temperature gradients as it was shown to be beneficial [WEN12].

As module testing is expensive, a common way in industry to evaluate the mechanical stability after soldering is to perform a ribbon pull test whereby the force to pull the ribbon is measured and the failure interface is examined. Unlike for electronic components there are no standards for pull test of soldered ribbons in PV. Looking at the natural load case of the cells in the module, a 180° angle pull angle may seem more realistic. However, it is more peeling than pulling. Pull test results have been reported at 45°, 90° [MON13], or at 180° [TJA10] pull angle thus it is needed to see if the same conclusions can be made for various pull angles.

In this thesis, we first evaluated a SALICIDE process sequence where sintering was performed after PVD Ni deposition. This required subsequent unreacted Ni removal and

thickening steps prior to Cu plating thus it was needed to understand parameters affecting adhesion between blanket plated layers. As we introduced laser patterning, self-aligned plating, and transferred the process to pilot-production tools we then had to evaluate the influence of laser processing and other cell processing steps on adhesion results. Some results have already been given in Chapter 5 and 6 since optimization of adhesion cannot go without addressing risks of junction damage. Additional results are presented below.

Adhesion of Ni/Cu/Ag plated contacts was evaluated by performing soldered ribbon pull tests and finger peeling tests. For the pull tests, a soldering flux Kester 925S was applied on the busbars and conventional tinned ($Sn_{62}Ag_{36}Pb_2$) copper ribbons (1.5x0.2mm^2, 70-90 N/mm^2 yield strength) from Ulbrich were hand soldered at ~280˚C unless mentioned otherwise. Cells were clamped on a free-moving X-Y table using a cell holder which can be modified to perform pull tests at 45, 90, or 135˚ pull angles. Ribbons were pulled using a manual pull tester (see Figure 7.1a). The force in newton was measured using a Chatillon DFA series force gauge and computed versus time using a Nexygen software. For the finger peeling tests (see Figure 7.1b), scotch tape was pressed by hand, at the cell edges, parallel to the plated fingers, peeled towards the busbars at a 180˚ angle, and the number of fingers taken off the cell surface was counted.

7.2.2. Adhesion between blanket plated layers

The adhesion failure interface is characteristic of the weakest interface thus it is important to address adhesion to Si but also between plated layers. In recent cell concepts with Ni/Cu plated contacts, attempts have been made to roughen Si surface chemically [KAR10] or by laser processing [WEN10] as to provide anchor points to improve adhesion. However, it is interesting to point out that a NaOH groove damage etch leaving relatively smooth Si surfaces was present in the process sequence of LGBC cells commercialized by BP Solar (see Chapter 3.2.7). The fact that early LGBC modules installed in 1992 in Toledo, Spain are still operational today [RUS12] provides evidence that long-term reliability is possible and that adhesion of Ni/Cu plated contacts can be sufficient when using an appropriate plating sequence. However, in LBGC cells the Ni/Cu plated contacts were buried in Si and hence it is not clear if good adhesion results can be achieved on smooth Si surfaces for non-buried Ni/Cu plated contacts.

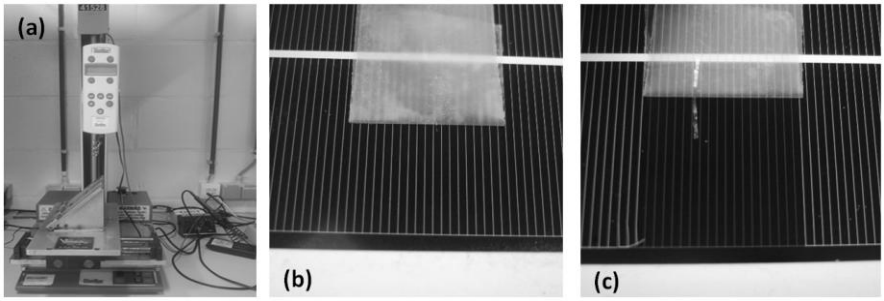


Figure 7.1: a) Photograph of manual pull tester setup with X-Y wafer clamping stage in position for 45˚ pull angle and Chatillon DFA series force gauge. Pictures of Ni/Cu/Ag plated contacts passing (b) and failing (non-optimized conditions) (c) a finger peeling test (i.e. scotch tape test).

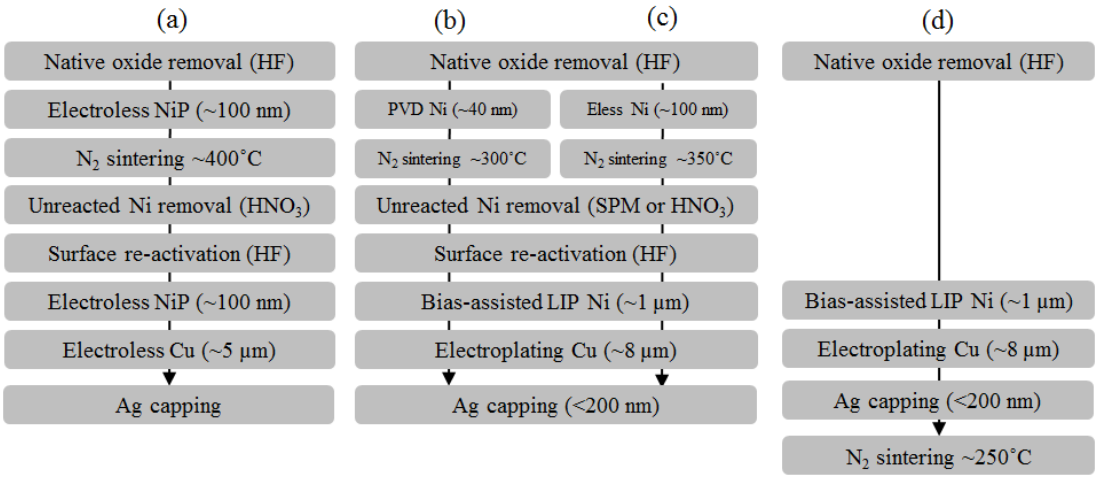


Figure 7.2: (a) Plating sequence used in BP Solar's LGBC cells [JEN03], (b) and (c) SALICIDE plating sequence with PVD Ni and electroless (Eless) NiP seed layers respectively, (d) simplified plating sequence (see Chapter 5).

The SALICIDE process sequence based on a thin PVD Ni or electroless NiP seed layer used in this thesis requires an HF step prior to Ni deposition and another HF step after unreacted Ni removal as indicated in Figure 7.2. We have mentioned that the first HF step is required to remove native oxide since it is known to inhibit nickel silicide formation (see Chapter 5.2).

To evaluate the importance of the second HF step after unreacted Ni removal, we used diode structures as shown in Figure 7.3. Such structures mimic the front metal stack, except for bias-assisted LIP Ni (1 µm) that is replaced by electroplating of Ni (for 1 µm), without being influenced by the patterning of the SiO_2/SiN_x. They also help visualizing surface hydrophobicity prior to electroless NiP (100 nm) and NiP surface coverage after deposition. For the former point, it was observed that a short water rinse (<30 sec) is preferred after native oxide removal in HF to prevent surface re-oxidation. Sintering was performed for 5 min at 400˚C under N_2, unreacted Ni was removed in 59% HNO_3 in 2 min, and in one case the subsequent 60 seconds 1% HF-dip was skipped prior to electroplating of Ni (1 µm) and Cu (8 µm).

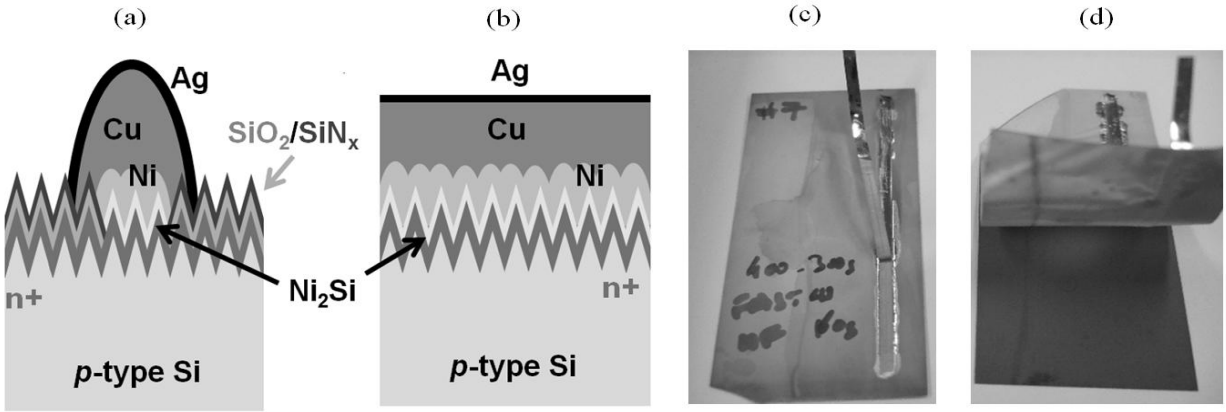


Figure 7.3: (a) Ni/Cu/Ag plated contact structure, (b) Diode structure mimicking the front side metal stack in (a), Pictures of soldered ribbon pull tests on plated diodes with (c) and without (d) HF-dip after unreacted Ni removal.

Soldered ribbon pull tests were performed at 45˚ pull angle and taking peak force values. For the samples where the second HF step was present, average values above 3.5N were obtained and the failure interface was found within the tinned copper ribbon (see Figure 7.3c). This is the preferred mode of failure showing that adhesion to silicon and adhesion between all plated layers is sufficient. This also demonstrates that with the correct plating sequence, a rough silicon surface is not required. The obtained peel force values when skipping the second HF step were virtually zero as the layers peeled off (see Figure 7.3d). Based on thickness measurements, the failure interface was identified at the silicide-nickel interface. As mentioned in Chapter 5.2, nickel silicide versus nickel selectivity of SPM and HNO_3 chemistries is based on the fact that oxidation and dissolution of unreacted Ni stops when a silicon oxide layer is formed on top of the silicide [CAR07]. It is presumed that this oxide layer needs to be removed (in HF) to obtain a strong silicide-nickel bond. Similar observations were recently published by Mondon et al [MON13] we showed that a 1s HF-dip after unreacted Ni removal was sufficient.

Knowing the importance of the first and second HF steps, we then evaluated the influence of additional process parameters on adhesion. We performed a trial following a design of experiment methodology and using diode test structures featuring a 0.6 µm deep 120 Ω/sq emitter as shown in Figure 7.3. We used a response surface central composite design with three factors: (i) electroless NiP thickness (20-120nm), (ii) sinter temperature T (270-400˚C), and (iii) sinter duration (15-120sec). Soldered ribbon pull tests were performed at 45˚ pull angle and peak force values recorded. The local ideality factor m at 0.4V was obtained from dark-IV measurements. Results as plotted for various sinter temperature and NiP thicknesses in Figure 7.4a as sinter duration was found to have little or no influence. The sintering temperature was found to be the main driver for adhesion with T<300˚C giving values <2N with often metal peel off at very low pull force values (see Figure 7.4b). Investigations performed in Chapter 5.3 revealed that little or no silicidation occurs with thin (<100 nm) electroless NiP layers for T<300˚C. Results presented here confirm that silicidation is required to obtain sufficient adhesion. To get adhesion values >3N resulting in wafer breakage (see Figure 7.4c) T>320˚C are required while T<340 ˚C are preferred to keep m<3.5. Therefore, the process window with alkaline electroless NiP for the present emitter depth is too narrow.

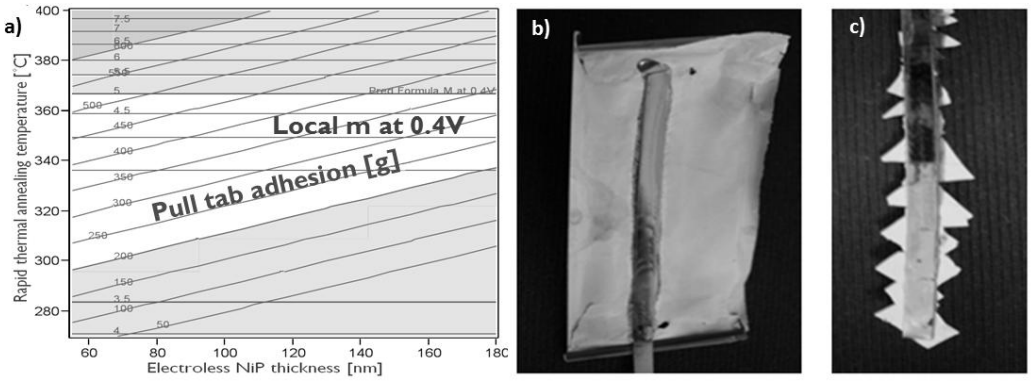


Figure 7.4: (a) Surface response of pull tab adhesion and local ideality factor m at 0.4V versus sintering temperature (T) and NiP thickness. (b) Metal peel-off for T<300˚C, (c) pull tab adhesion >3N (wafer breakage) for T>320˚C.

7.2.3. Influence of cell processing

New tests were designed to evaluate the influence of ps-UV laser ablation on adhesion as results obtained with diode structures did not incorporate the effect of laser ablation. Alkaline textured p-type CZ wafers were processed into full Al-BSF solar cells featuring a SiN_x ARC. The front ARC was patterned using ps-UV laser ablation. Self-aligned Ni/Cu/Ag plated contacts were obtained following the sequence described in Figure 7.2a. For these tests, sintering was performed at 350˚C for 2min. The line spacing in the busbars was varied from 10 µm to 40 µm as shown in Figure 7.5. As a control, the same conditions were applied on diode structures where ps-UV ablation was directly performed on Si. Ribbons were hand soldered continuously or in spots (~1 cm long). Ribbon pull tests were performed at 45˚ pull angle taking peak force values.

Line spacing in the busbars was found to have a strong influence on adhesion results. The best results were obtained for 10 µm spacing (~100% contact area) with adhesion values being limited by wafer breakage (see Figure 7.5a). For 20 or 40 µm spacing, the failure interface was found within Si with pull force values well below 2N (see Figure 7.5e). Measured values were lower with continuous soldering, as it generates more stress, than with spot soldering. Nevertheless, adhesion values above 2.5N were obtained with continuous soldering on the control diode samples (100% contact area in all cases) independently of line spacing thus providing no evidence that laser ablated surfaces are inherently weak. The hypothesis for the adhesion failure mechanism of cells is that stress is distributed over fewer contact points as the line spacing in the busbars is increased. This leads to Si microcracks generation and propagation at low pull force values thus explaining the failure interface being in silicon. It should also be mentioned that fast cool downs (as it is the case here with hand-soldering) and too high soldering temperatures have been observed to lead to similar Si micro-fracturing with screen printed Ag contacts [HAR12]. Higher adhesion values may be measured using a pull tester that minimizes micro-crack propagation during ribbon pulling as presented in [WEN09]. However, this is only useful if it correlates well with module failure during environmental testing.

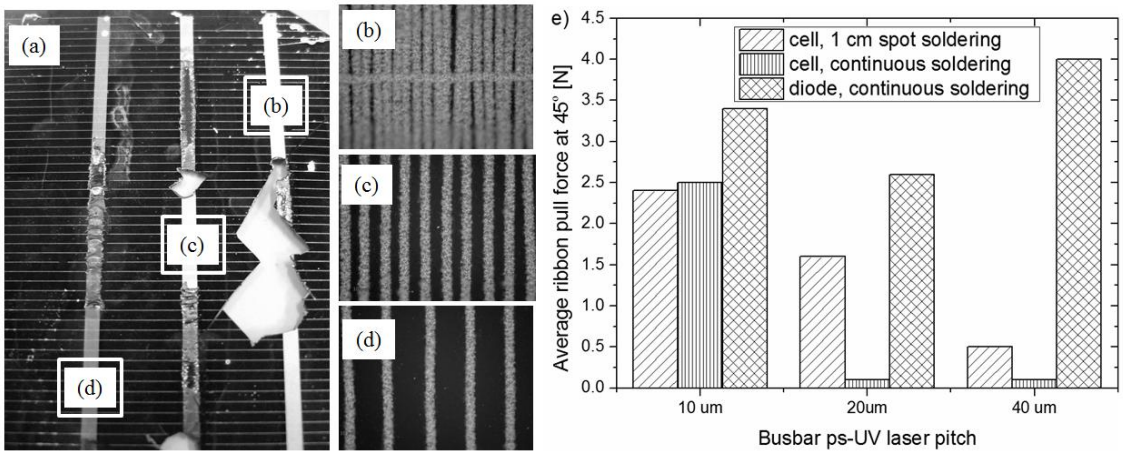


Figure 7.5: (a) Solar cell sample after 45˚ ribbon pull test in busbars with 10 µm (b), 20 µm (c), and 40 µm (d) line spacing. (e) Average 45 ˚ ribbon pull force values for various line spacing and soldering conditions.

Following these results, new design of experiments (DOE) were performed to evaluate the influence of ps-UV laser ablation parameters in combination with Ni sintering conditions. Large area (12.5x12.5 cm^2) p-type CZ-Si wafers were processed into full Al-BSF solar cells featuring a 1 µm deep 120 Ω/sq emitter. Prior to rear Al screen printing, a resist was applied on the front side to protect the SiO_2/SiN_x DARC, the rear thermal oxide was removed in HF, and the resist was removed in acetone followed by isopropyl alcohol and de-ionized water rinse. After Al BSF formation (firing at ~800˚C peak wafer temperature), four mini-cells (5x5 cm^2, 2x 1.5mm wide busbars) per wafer were patterned in the front DARC using either ps-UV laser ablation (10 µm line spacing in busbars) or a wet etching photolithography sequence (see Chapter 3.2). A Ti/Cu lift-off sequence (see Chapter 5.1) was used as control. A ½ factorial with center points DOE was performed for ps-UV laser samples using five factors: (i) PVD Ni thickness (40, 100, 160 nm), (ii) sintering temperature (275, 300, 325˚C), (iii) sintering duration (30, 60, 90s), (iv) mean laser power (65, 85, 100mW), (v) pulse overlap (0, 25, 50%). A full factorial with center points DOE was performed for the wet etched samples using the same PVD Ni sintering matrix. Ribbon pull tab force values were measured at 45˚ after spot soldering at 280˚C. Junction damage was evaluated from pseudo-fill factor (pFF) measurements on finished devices.

Complete DOE matrices are given in Appendix C together with sorted parameter estimates. From these results the following observations could be made.

<u>For wet etched samples:</u>

- Mean adhesion values >2.5N for all conditions tested.
- Lower pFF values for higher sintering duration, higher sintering temperatures, and lower Ni thickness.

<u>For ps-UV laser ablated samples:</u>

- Mean adhesion values <2N for all conditions tested. Lower Ni thickness, higher laser pulse overlap, and higher pulse overlap x pulse energy were found to have a significant impact on increasing adhesion values. Sintering time and temperature were not significant for adhesion within the range of parameters tested.
- pFF>82% (comparable to Ti/Cu reference process) were found for all conditions tested.

In summary, these results demonstrate that the plating sequence with a thin PVD Ni seed layer described in Figure 7.2b in combination with a 1 µm deep 120 Ω/sq emitter provides sufficient busbar adhesion and good electrical results for wet etched samples. It was observed that low sintering temperatures and short sintering duration (e.g. 275˚C for 30s) give higher pFF. For ps-UV laser ablated, further investigations revealed that the conditions tested did not provide uniform ablation of SiO_2/SiNx DARC layers. As suggested here, pulse overlap and mean laser power were increased and results were discussed in Chapter 6.2.

Following these tests, the process sequence was simplified by first replacing the thin PVD Ni seed layer by a thick (~1 µm) bias-assisted LIP Ni and then moving the sintering at the end of the Ni/Cu/Ag plating sequence (see Figure 7.2d). In both cases, equivalent adhesion and pFF results could be demonstrated and the results were presented in Chapter 5.4.3.

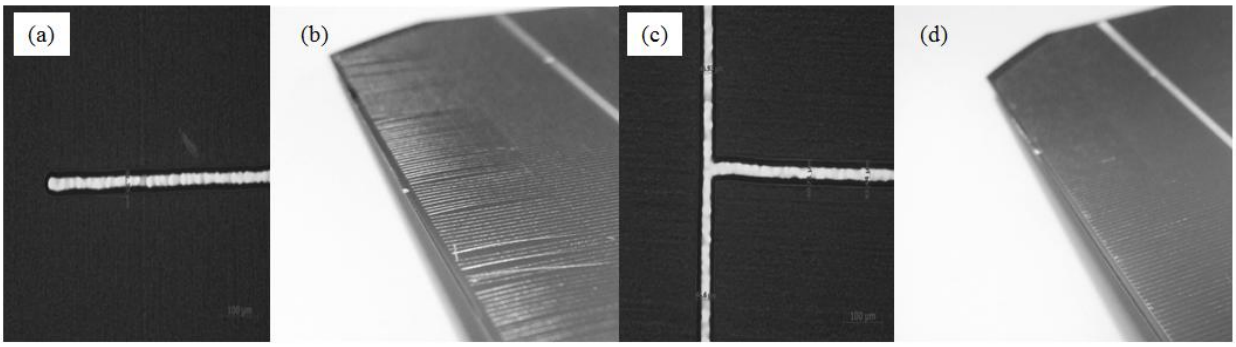


Figure 7.6: (a) Optical microscope of finger without edge pinning line. (b) Picture of solar cell without edge pinning line. (c) Optical microscope of finger with edge pinning line. (d) Picture of cell with edge pinning line.

Finally, the influence of the ps-UV laser pattern on adhesion of Ni/Cu/Ag plated fingers was looked at by performing finger peeling tests. During plating it was sometimes observed that the plated finger extremities would curl upwards due to tensile stress in Cu (see Figure 7.6a and b). The addition of a pinning line at the edge as shown in Figure 7.6c together with optimized ps-UV laser ablation parameters were found to resolve this issue and cells passed finger peeling tests (see Chapter 6.2). Similar observation were made with wet etched samples and consequently a pinning line was added to photolithography masks. It is speculated that the addition of a pinning line increasing the stress values above which delamination would initiate.

7.2.4. Influence of plating chemistries

As electroplating of nickel is performed for a wide range of applications other than PV it is interesting to look at the influence of electrolyte composition and operating conditions on the properties of the deposits. Results presented so far were obtained using a sulphamate bath from DOW for bias-assisted LIP Ni. As we installed the MECO plating tool, early tests were performed using a sulfate nickel bath (PV80) from OMG electronic chemicals. “Watts” Ni baths (named after Prof. Oliver P. Watts) are very common for decorative applications in industry and have been used for bias-assisted LIP Ni in PV [BAR12, MON13]. The composition of the three different nickel electrolytes are summarized in Table 7.1. The points addressed below are mainly adapted from a book chapter on electrodeposition of nickel by G.A. di Bari [diB00].

“Watts” Ni baths contain nickel sulfate (source of Ni ions), nickel chloride, boric acid, and wetting agents (also called surfactants). Nickel chloride serves primarily to improve anode corrosion, thickness uniformity, and also increase electrolyte conductivity. However, excessive amounts increase internal stress. As with electroless NiP solutions, boric acid is mainly used as pH buffer. In Watts baths, hardness, tensile strength, and internal stress increase strongly above pH 5. Wetting agents are added to lower the surface tension of the plating solution so that air and hydrogen bubbles do not get attached to the surface being plated and hence prevent pitting and voids formation. Deposition temperatures around 55˚C are preferred as lower and higher

temperatures have been reported to increase internal stress. Nickel electrodeposited from additive-free Watts solution exhibit internal tensile stress in the range of 125-185 MPa.

The nickel sulfate bath described in Table 7.1 is mainly based on nickel sulfate and boric acid. Because the electrolyte does not contain any chloride, sulfur-containing nickel pellets (S-Nickel) are required as anode material to enable dissolution and hence Ni replenishment. The sulphur in the pellets (~0.02%) does not enter solution but forms insoluble nickel sulfide that is retained in the anode bag where it acts to remove unwanted copper impurities from the plating solution. The bath also contains sodium sulfate which strongly increases the throwing power of the electrolyte (i.e. ability to plate uniformly in prominent and recessed areas) and additives to improve leveling (i.e. smooth uniform finish). Internal tensile stress in the range of 120 MPa have been reported for all sulfate baths (i.e. without sodium sulfate).

Nickel sulphamate baths typically enable deposits with lower internal tensile stress in the range of 0-55 MPa. They can be operated at lower temperature and at higher current densities because of the high solubility of nickel sulphamate enabling a higher Ni metal concentrations that other nickel electrolytes. However, for bias-assisted LIP Ni, Ni metal concentration cannot be too high since this would lead to poor light transmission. A small amount of nickel chloride is usually present as to enable dissolution of the Ni anode. The need for nickel chloride can be eliminated by using S-Nickel pellets thereby enabling a reduction in internal stress and also preventing Al dissolution [diB00]. Finally, as with other nickel electrolytes, sulfur-containing organic additives can be added to reduce internal stress or even make it compressive.

Table 7.1 Composition and operating conditions of nickel sulphamate and sulfate electrolytes used for bias-assisted LIP Ni in this thesis as compared to a typical "Watts" nickel electroplating solution [BAR10]. Proprietary additives are also present in the bias-assisted LIP Ni electrolytes which are not mentioned in this table.

	Sulphamate	Sulfate	"Watts"
Nickel metal (g/L)	30	20	50-90
Nickel chloride (g/L)	2	-	30-60
Boric acid (g/L)	40	30	30-45
pH	4.0	4.4	2-4.5
Temperature (˚C)	38	55	44-66

Nickel sulphamate: $Ni(SO_3NH_2)_2 \cdot 4H_20$ (180 g/L Ni), Nickel sulfate: $NiSO_4 \cdot 6H_20$ (1g/L increases Ni content by 0.22g/L), Nickel chloride: $NiCl_2 \cdot 6H_20$ (1g/L increases Ni content by 0.25g/L), Boric acid, H_3BO_3

As the MECO plating tool was installed, qualifications tests, including ribbon pull tests, were conducted. The "imec" simplified plating sequence (see Figure 7.1d) consists of: (i) HF clean, (ii) bias-assisted LIP Ni, (iii) electroplating of Cu, (iv) immersion Ag capping (i-Ag). An additional bias-assisted LIP Cu is present prior to electroplating of Cu in the MECO tool and the Ag capping is performed by electroplating. In addition, all plating chemistries present in the MECO tool for these acceptance tests were different than the chemistries used in the imec plating sequence. After ps-UV laser ablation and Ni/Cu/Ag plating, the 15.6x15.6cm^2 cells were

sintered for 4 min at 250˚C, ribbons were spot soldered (~1 cm) by hand at 280˚C, and ribbon pull tests were performed at 45˚ pull angle taking peak force values. Pull force values >2N were measured for cells plated with the reference imec sequence while cells plated in the MECO tool gave ~1N (see Figure 7.7a). Doing only the bias-assisted LIP Ni step in the MECO tool (sulfate bath) followed by i-Ag capping in a beaker and sintering we found no adhesion (see Figure 7.7b) while ~2.7N were obtained with the "imec" bias-assisted LIP Ni in a beaker (sulphamate bath). All other steps (e.g. ps-UV laser ablation, HF pre-cleaning) and Ni deposition parameters (deposition time, rear applied potential) were identical. It is speculated that improved adhesion values are the result of lower internal tensile stress of the Ni layers deposited in the sulphamate bath as compared with Ni deposited in the sulphate bath. Finally, replacing the sulfate bath by the sulphamate one in the MECO tool we could demonstrate with the full Ni/Cu/Ag stack equivalent pull force results ~2N, as shown in Figure 7.7c. This demonstrates that the Ni sulfate bath present initially in the MECO tool was solely responsible for the worse adhesion results.

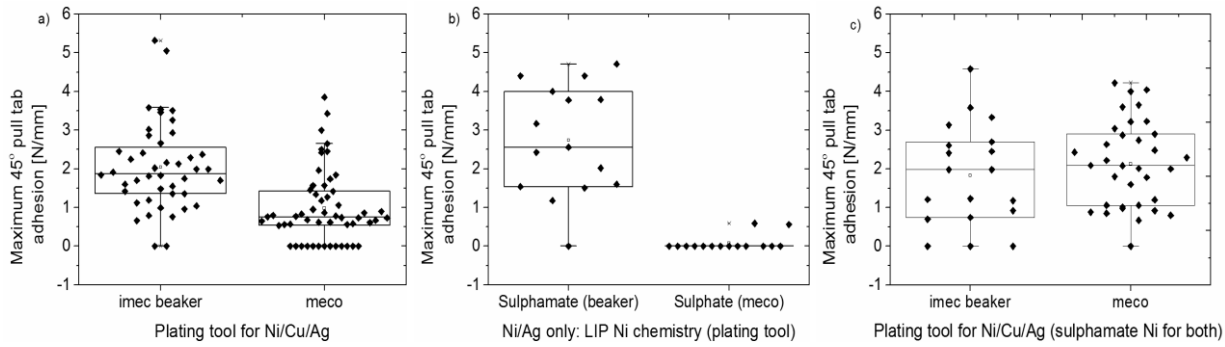


Figure 7.7: Maximum ribbon pull force values at 45˚ normalized to the busbar width (1 mm) for: (a) Ni/Cu/Ag plated contacts with imec sequence (Ni sulphamate) or in MECO tool (Ni sulphate), (b) various Ni chemistries + immersion Ag, (c) Ni/Cu/Ag contacts with imec sequence or in MECO tool using Ni sulphamate. In all cases, sintering was done prior to soldering.

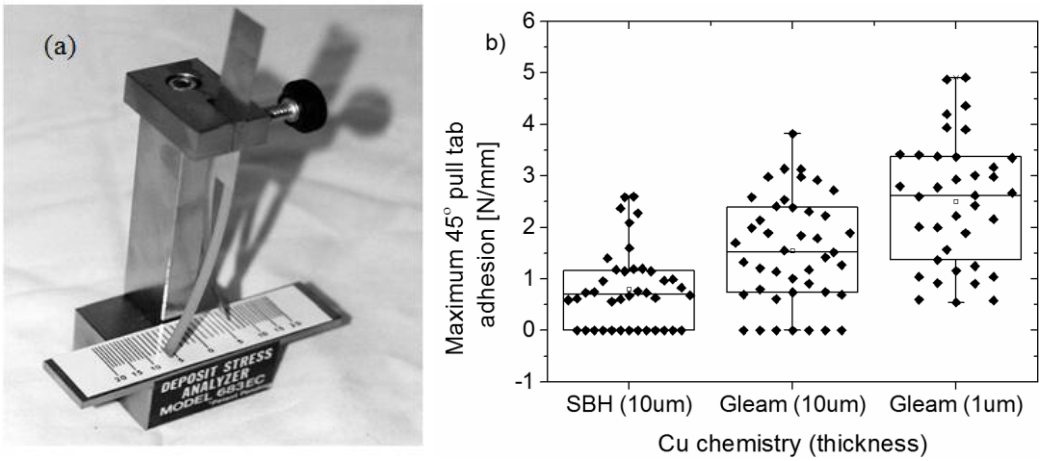


Figure 7.8: (a) Picture of bent strip used to measure internal stress [RIC97] (b) Maximum ribbon pull force values at 45˚ normalized to the busbar width (1 mm) for Ni/Cu/Ag plated contacts with imec sequence for various Cu chemistries (see text) or Cu thicknesses. Ni and immersion Ag thicknesses are 1 μm and 0.2 μm respectively.

For bias-assisted LIP Ni layers, experiments were conducted to extract internal stress from the curvature of 2mm wide strips laser-diced (around the busbar) from plated cells. However, measurements were found inconclusive as reproducibility was poor and both rear Al and dielectrics layers were found to affect wafer curvature. Internal stress measurements from bent strips have also been performed. If the test strip legs (see Figure 7.8a) are spread outward on the side that has been plated (plated side out and resist side in) the deposit stress is tensile in nature and vise-and-versa for compressive stress. The leg deviation from the center can then be measured using a scale and the internal stress calculated according to [RIC97]:

$$S = \frac{UKM}{3T} \tag{7.2}$$

where S is the internal stress in pounds per square inch, U is the number of increments spread, T is the deposit thickness in inches, K is the strip calibration constant (provided with test strips), and M equals the modulus of elasticity of the deposit divided by the modulus of elasticity of the substrate material. The internal stress can be converted to MPa by dividing S by 145.

The fact that bent strips need to be electrodeposited means that further work is needed to demonstrate that measured internal stress corresponds to internal stress in bias-assisted LIP Ni layers. For this reason, bent strips measurements were continued with electrodeposited Cu. Using stress relieving additives (DOW SBH bath), internal stress could be measured at 0 MPa using the bent strips as opposed to 7 MPa for "imec" standard Cu gleam chemistry. However, this did not yield higher pull force values for comparable Cu thicknesses (see Figure 7.8b). Possibly, internal stress changes during silicidation and/or with soldering or the low internal stress values as compared to Ni layers are not significant to affect adhesion. Therefore, further characterization is required to clarify these aspects. Nevertheless, the low stress Cu plating bath is already an attractive solution for back-contact cells where thick (>20 μm) Cu layers are required without inducing any wafer bow. Finally, the fact that higher pull force values were obtained for thin (~1 μm) Cu layers indicates that multi-busbar approach (see Chapter 3.3) could benefit from better adhesion as Cu thickness is reduced.

In summary, these results demonstrate that plating chemistries may influence adhesion results thus the deposit properties can be engineered to maximize adhesion values.

7.2.5. Influence of measurement methods

At the beginning of this Chapter it was mentioned that ribbon pull test results have been reported at various pull angles (e.g. 45˚, 90˚, and 180˚) and that peak force values may be misleading as average values can be much lower. These two aspects were evaluated by performing ribbon pull tests on 15.6x15.6cm^2 cells Ni/Cu/Ag plated in the MECO tool (sulphamate Ni bath) and sintered at 250˚C for 4min. All cells used for this experiment gave efficiencies above 20%. Ribbons were hand soldered at 325˚C either in spots (~1 cm) or continuously. The cell holder was modified to enable 45, 90, or 135˚ pull angles. Measurements were taken using maximum pull force values or integrating pull force values versus time .

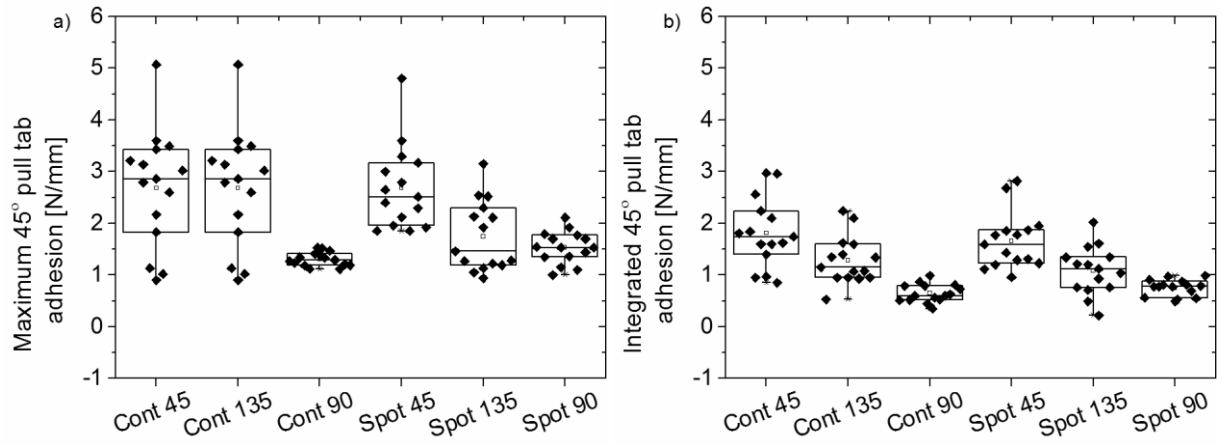


Figure 7.9: (a) Maximum and (b) average (i.e. integrated) ribbon pull force values at various angles for Ni/Cu/Ag contacts plated in the MECO tool and sintered in the BTU tool. In all cases, ribbons were continuously or spot (standard) soldered at 325˚C by hand.

Taking maximum pull force values we found ~2.5N at 45˚ pull angles either with continuous or spot soldering (see Figure 7.9a) which is comparable with results given so far. As reported by others [MON13], 90˚ pull angles appears to be the most stringent test with values dropping to ~1.5N. Comparing these results with average (i.e. integrated) pull force values, the same trends with pull angles are observed, as shown in Figure 7.9b. However, values are about 1N lower which confirms the general statement that average pull force values are lower than peak force values. Nevertheless, in all cases pull force values are limited by wafer breakage.

In summary, rather than defining a minimum pull force value as being "sufficient", it should be mentioned that one decisive (rather "minimum") criteria is being able to demonstrate that modules with Ni/Cu/Ag plated cells can pass environmental testing.

7.3. Thermal cycling and damp heat testing

7.3.1. Introduction

Typically the most stringent IEC61215 tests are the environmental tests which consists in temperature cycles (TC), damp heat (DH), and humidity-freeze (HF). There are five "major visual defects" and six operational "pass/fail" criteria [ARN13]. One of this operational "pass/fail" criteria is that the max. power (P_{max}) should not be less than 95% of the initial P_{max}.

For TC200 (200 cycles), the module is subjected to temperature cycles between –40°C± 2°C and +85°C±2°C with the profile given in Figure 7.10a. A current within ±2% of the current measured at peak power (I_{mp}) is injected when the module temperature is above 25°C. TC challenges mainly the soldered connections due to the different CTE of the various encapsulated materials which may result in visual or operational failure. Failure rates can be up to 40%.

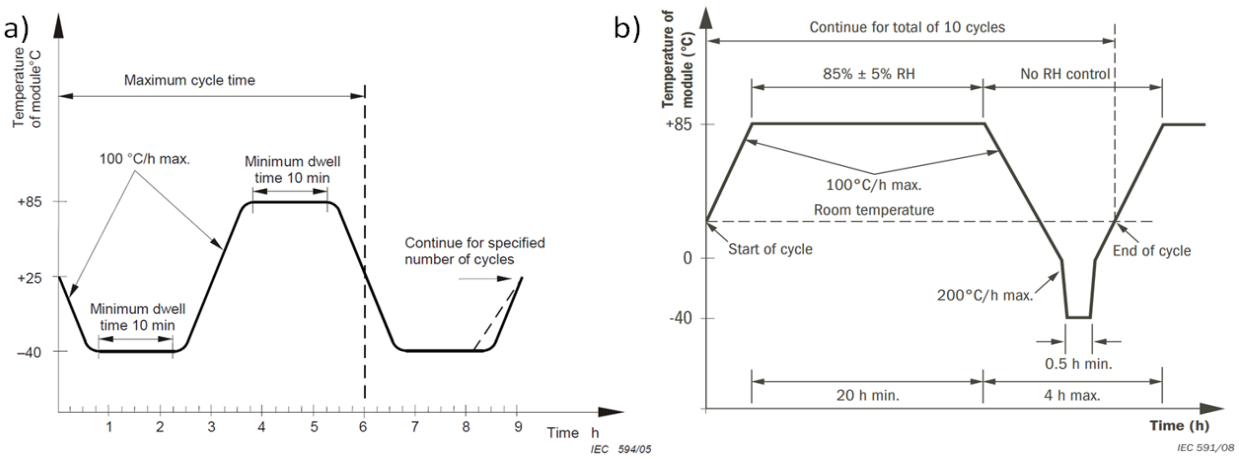


Figure 7.10: a) IEC61215 thermal-cycling profile. b) IEC61215 humidity–freeze profile.

For DH1000 (1000 hours), the module is subjected to 85°C±2°C with a relative humidity (RH) of 85% ± 5% for 1000 hours. This test mainly determines the ability of the module to withstand penetration of humidity, particularly at the module edges, which may lead to important delamination and corrosion of cells parts. For cells with Ni/Cu/Ag plated contacts, this test also challenges the ability to withstand Ni or Cu diffusion which may lead to P_{max} degradation or discoloration of the encapsulant material. Failure rates can be up to 50%.

For HF, the module is subjected to 10 complete cycles following the profile given in Figure 7.10b. The ability of the module to withstand the effects of high temperatures combined with humidity (85°C±2°C with RH=85% ± 5%) followed by extremely low temperatures is tested. Soldered connections are mainly challenged and failure rates can be up to 20%.

In this thesis, more stringent extended TC and DH testing were conducted on i-PERC cells featuring Ni/Cu/Ag contacts plated using the simplified sequence described in Figure 7.1d. A batch of large area (12.5x12.5 cm^2), p-type, m-CZ-Si wafers was processed into i-PERC featuring a 1µm deep 120 Ω/sq emitter. To enable conventionally soldering at both side, some cells additionally received Al/Ni/Cu (2µm/40nm/150nm in one sputtering sequence) after rear Al contact firing and prior to front ps-UV laser ablation. All cells were Ni/Cu/Ag plated using single wafer equipment (i.e. "imec" sequence and not MECO plating) and sintering was performed at 250˚C for 4min in a single wafer sintering tool (AccuThermo AW 610 from Allwin21 Corp.). Average efficiencies around 20% were obtained on 74 cells with the best cell giving j_{sc}=38.8mA/cm^2, V_{oc}=661mV, FF=79.2%, and ŋ=20.3% (confirmed by ISE Callab).

For testing purposes, some of these cells were then tabbed front and rear either by spot soldering (~320ºC) at 5 points along the cell length or using a non-Ag containing electrically conductive adhesive (ECA) film from Hitachi Chemical. In the latter case, a thin ECA film was placed between the cell and ribbon and continuous front and rear contacts were simultaneously formed at 180ºC and 2MPa pressure. The conductive adhesive film enabled direct contact to be made to the rear Al of standard i-PERC cells. Ribbon pull tests were performed at 45º pull angle and maximum pull force values were normalized to the metallized contact width (N/mm).

Ribbon pull tests results are presented in Table 7.2. For the front side, comparable values ~2-2.5N/mm were obtained with soldering or with ECA. Cohesive failure within the ECA was observed while soldering resulted in the typical wafer breakage. Cohesive failure within the ECA was also observed at the rear side with pull force values ~3N/mm. Excellent pull force values of 3.5N/mm, with cohesive failure in the ribbon, were obtained for hand soldering on the rear sputtered Al/Ni/Cu. Finally, finger peel tests were performed using scotch tape on several cells for both Ni/Cu/Ag plated and the screen-printed Ag control cells and no failure was observed.

Table 7.2 Ribbon pull tests at 45º pull angle. Ag screen printed (Ag-SP), ECA: electrically conductive adhesive

Front contact type	Rear contact type	Tabbing technology	Measurements per side	Average front [N/mm]	Average rear [N/mm]
Ag-SP	i-PERC Al	ECA	20	2.5	2.9
Ni/Cu/Ag	i-PERC Al	ECA	50	2.2	3.3
Ni/Cu/Ag	i-PERC Al	soldering	50	2.5	NA
Ni/Cu/Ag	i-PERC Al +Al/Ni/Cu/Ag*	soldering	20	2	3.5

*Only Al/Ni/Cu were additionally sputtered, the rear Ag is obtained during immersion Ag plating of front contacts.

Following these results, cells were pre-conditioned to approximately 5kWhr/m^2 to remove any light induced degradation before testing. Eighteen 25x25cm^2 single cell laminates (tedlar/EVA/cell/EVA/glass) were prepared with either conventional soldering or ECA using the conditions mentioned above. The single cell laminates were put on either TC or DH at imec. For TC at imec, no current was applied and hence the test does not replicate exactly IEC61215. In addition, two modules were made (size for 60x 15.6x15.6 cm^2 cells), one for TC and the other for DH, and put on test at external IEC61215 credited test site. Within each module, there were five individual cell strings consisting of 8 or 10 cells. Each string was electrically separated from the others to allow all strings to be measured individually. For both single cell laminates and the cell strings, different cell type/tabbing technology combinations were tested and screen printed Ag i-PERC cells were used as control. All different combinations are summarized in Table 7.3.

Table 7.3 Cell type/tabbing technology combinations for single cell laminates and strings in modules on test.

Front contact type	Rear contact type	Tabbing technology	#laminates for DH	#laminates for TC	#cell strings for DH	#cell strings for TC
Ag-SP	Al-BSF	soldering	2	2	1	1
Ag-SP	i-PERC Al	ECA	2	2	1	1
Ni/Cu/Ag	i-PERC Al	ECA	2	2	2	2
Ni/Cu/Ag	i-PERC Al Al/Ni/Cu/Ag	ECA	2	2	1	1
Ni/Cu/Ag	i-PERC Al +Al/Ni/Cu/Ag	soldering	1	1	-	-

7.3.2. Results

Measurements were performed at regular interval during damp heat (DH) and thermal cycling (TC) testing of both single cell laminates and modules with 10 cells strings. Percentage changes in j_{sc}, V_{oc}, FF and power (P_{max}) as a function of cycles or hours in DH can be found in a joint publication by Russell et al. [RUS12]. Main results are summarized below in Table 7.4 and Table 7.5. As we could not measure any significant differences between cells tabbed with conventional soldering or using ECA, results were lumped together under either Ni/Cu/Ag plated front contacts or screen printed Ag front contacts. The screen printed Ag i-PERC cell string (ECA tabbing) which failed after 50 thermal cycles was excluded from the averages in Table 7.5. Electroluminescence images showed three broken cells in this string before thermal cycling.

Table 7.4 : Summary of damp heat (DH) and thermal cycling (TC) reliability results for single cell laminates

# single cell laminate type		IEC61215		Extended IEC61215	
		TC200	DH1000	TC300	DH1500
Ni/Cu/Ag: 4x ECA 1x soldering	Avg Δj_{sc}	-0.1%	-2.7%	-0.5%	-2.6%
	Avg ΔV_{oc}	-0.3%	1%	0.2%	1.1%
	Avg ΔFF	-0.9%	0.9%	-0.8%	1%
	Avg ΔP_{max}	-1.3%	-0.8%	-1.3%	-0.5%
	Max ΔP_{max}	-2.2%	-4.1%	-2.3%	-4.6%
Screen printed Ag: 2x ECA 2x soldering	Avg Δj_{sc}	-0.1%	-1.2%	-0.2%	-0.9%
	Avg ΔV_{oc}	0.1%	0.3%	0.2%	0.4%
	Avg ΔFF	-0.8%	-0.7%	-0.9%	-1.1%
	Avg ΔP_{max}	-0.8%	-1.6%	-1.0%	-1.5%
	Max ΔP_{max}	-1.4%	-2.8%	-1.6%	-2.5%

Table 7.5 Summary of damp heat (DH) and thermal cycling (TC) reliability results for 10 cell strings.

# cell string type		IEC61215		Extended IEC61215	
		TC200	DH1000	TC300	DH1500
Ni/Cu/Ag: 3x ECA	Avg Δj_{sc}	2.9%	2%	2.4%	1.6%
	Avg ΔV_{oc}	0.2%	1.2%	0.5%	0.4%
	Avg ΔFF	-1.2%	-0.6%	-3.2%	-2.9%
	Avg ΔP_{max}	-1.3%	-0.8%	-1.3%	-0.5%
	Max ΔP_{max}	-2.2%	-4.1%	-2.3%	-4.6%
Screen printed Ag: 1x ECA 1x soldering	Avg Δj_{sc}	1.6%	1.7%	0.5%	1.5%
	Avg ΔV_{oc}	0.2%	0.3%	0.2%	0.3%
	Avg ΔFF	-0.8%	0.5%	-0.7%	-0.4%
	Avg ΔP_{max}	0.9%	2.3%	-0.2%	1.5%
	Max ΔP_{max}	0.9%	1.8%	-0.2%	0.7%

Many of the single cell laminates on DH testing showed significant progressive j_{sc} loss dominating cell efficiency losses particularly for the Ni/Cu/Ag plated cells as shown in Table 7.4. These laminates had obvious EVA discoloration and were tinted brown. As this affected both cell laminates with screen printed Ag or Ni/Cu/Ag plated contacts and no such j_{sc} loss was seen with cell strings under DH testing, the cause is believed to be related to the batch of EVA or tedlar used for the single cell laminates.

As mentioned earlier, one of the critical IEC61215 "pass/fail" criteria is that the maximum power (P_{max}) should not be less than 95% of the initial P_{max} criteria after TC200 or DH1000. This criteria could be demonstrated, even extending the tests 1.5x, for all single cells laminates and 10 cells strings (except the Ag i-PERC cell string for TC with cracked cells) on test. More variation in P_{max} results between 1 cell laminates and 10 cell string of the same type were observed than between screen printed Ag and Ni/Cu/Ag plated results. Therefore, this work provides no statistically based evidence for any performance difference between screen printed Ag and Ni/Cu/Ag plated front contacts on DH or TC testing up to 1.5x IEC61215.

In summary, we could demonstrate that cells featuring a simplified sequence to define Ni/Cu/Ag plated contacts could pass some of the most stringent environmental module testing. This was one of the main objectives of this thesis. However, this is just a first step as any changes in the process sequence requires tests to be repeated. Ultimately, and as mentioned at the beginning of this Chapter, complete IEC61215 testing or even extended module testing should be performed on a regular basis with full size 60 cells modules to demonstrate that Ni/Cu/Ag plated contacts can pass the "minimum" requirements until reliability standards are defined.

7.4. Accelerated thermal ageing

7.4.1. Introduction

Copper is the fastest diffusing 3d transition metal in Si and Cu diffusion can be significant even at room temperature (see Chapter 3.2.4). Cu diffusion in Si leads to formation of Cu precipitates or complexes that can be electrically active, particularly in n-type material, and hence Cu is also known as a "lifetime-killer". Therefore, diffusion barrier(s) that can withstand subsequent processing steps and ensure long-term reliability are required in devices with Cu contacts. In the previous section, we demonstrated that solar cells featuring a simplified sequence to define Ni/Cu/Ag plated front contacts could withstand the 250˚C annealing step performed at the end followed by 1500 hours at 85˚C (encapsulated cells). However, this does not guarantee long-term reliability as significant Cu diffusion may occur over the lifetime of the module (20+ years) particularly when modules are placed in hot climates (40-55°C continuous operation, with maximum temperatures of 75°C) [KUR11] or subjected to hot spots.

The simplified sequence to define Ni/Cu/Ag plated front contacts results in hemispherical contacts with Cu being present on top of both the Ni contact/barrier and the front dielectric(s) (see Chapter 5.4.3). Unwanted Cu deposition may also occur in pinholes/scratches present in the front dielectrics ("parasitic plating") or on the rear aluminum surface. Cu diffusion into Si will

depend on the properties of each of these layers which can be affected by the deposition methods used or the process sequence (e.g. inter-diffusion of Ni and Cu during sintering at the end).

Rather than determining diffusion coefficients for each of the layers individually, the approach followed was to determine experimentally the time t required to reach 95% of the original pFF when submitting solar cells to thermal stress and correlating it to Cu diffusion according to [BAR11]:

$$t = \frac{L^2}{D_0 \exp\left(\frac{-E_a}{kT}\right)} \tag{7.2}$$

with L the diffusion depth, k the Boltzmann constant, T the temperature, and the activation energy E_a and constant D_0 represent diffusion via the weakest part (i.e. fastest diffusion path). Equation (7.2) can be re-written as:

$$\underbrace{\ln(t)}_{y} = \underbrace{E_a}_{a} \cdot \underbrace{\frac{1}{kT}}_{x} + \underbrace{\ln\left(\frac{L^2}{D_0}\right)}_{b} \tag{7.3}$$

The failure times t for various temperatures can be fitted by a linear function if the diffusion parameters (E_a and D_0) and the depth required to reach 95% of the original pFF depth (i.e. L) remain the same. This allows to extrapolate the failure time at operating conditions (e.g. 55˚C). However, the method does require solar cells to fail which may not happen even after more than 1000 hrs. at 225˚C as observed by Bartsch in his thesis [BAR12]. Similar observations were made in this work as Ni/Cu/Ag (1.3/9/0.3 µm) plated cells solar cells featuring a 1 µm deep emitter did not fail even after 3500 hrs. at 200˚C (see Figure 7.11a). For this reason, accelerated thermal ageing tests were performed at elevated temperatures (200˚C, 300˚C, 350˚C, and 400˚C) and we compared: (i) different Ni barrier thicknesses (0.3 µm, 0.6 µm, 1.3 µm) and (ii) two different emitter profile (1 µm 120Ω/sq and 0.5 µm 80 Ω/sq). Cu and Ag thicknesses were kept constant at 9 µm and 0.3 µm respectively. Controls groups with Ni/Ag (1.3/0.3 µm) were also included. All groups, except another control group with screen printed Ag contacts (156mm cell) included at least 4 mini-cells (5x5cm^2) and were sintered at 250˚C for 4min (standard annealing sequence) prior to thermal ageing tests

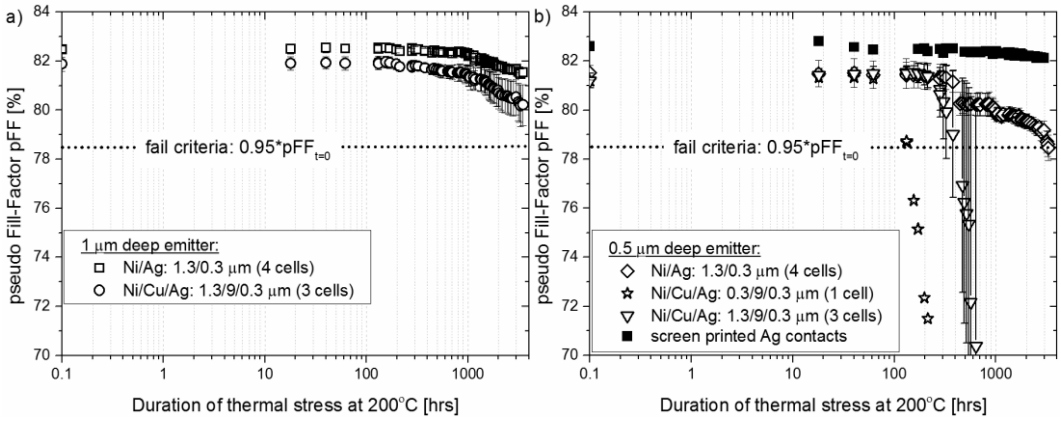


Figure 7.11: Measured pseudo fill factor as function of thermal stress duration at 200˚C for (a) cells featuring a 1µm deep 120Ω/sq emitter and (b) cells featuring a 0.5µm deep 120Ω/sq emitter

7.4.2. Results

Elevated temperatures (>250˚C) complicate the analysis as several effects may occur concurrently. On one hand, failure could occur due to nickel silicide and/or nickel reaching the junction and not only due to Cu diffusion. On the other hand, nickel silicide formation during thermal ageing may well slow down Cu diffusion (thicker nickel silicide barrier) thus making the extrapolation at operating conditions (no extra silicide formation) invalid.

Ni barrier thickness appears to control the time to failure with thin Ni barriers failing faster as shown in Figure 7.12. This implies that nickel silicide formation is not controlling time to failure since if it was the case all samples would fail at the same time. This is because complete NiSi formation at 400˚C would consume a 0.5µm junction in all samples (Si consumption: 1.83xNi thickness, see Chapter 3.2.5). The trend with Ni barrier thickness also implies that front dielectrics are not the weakest point to Cu diffusion. This is supported by the fact that samples with only Ni/Ag generally failed faster than samples with Ni/Cu/Ag: 1.3/9/0.3 µm meaning that having Cu on dielectrics is not worse than having Ni on Si.

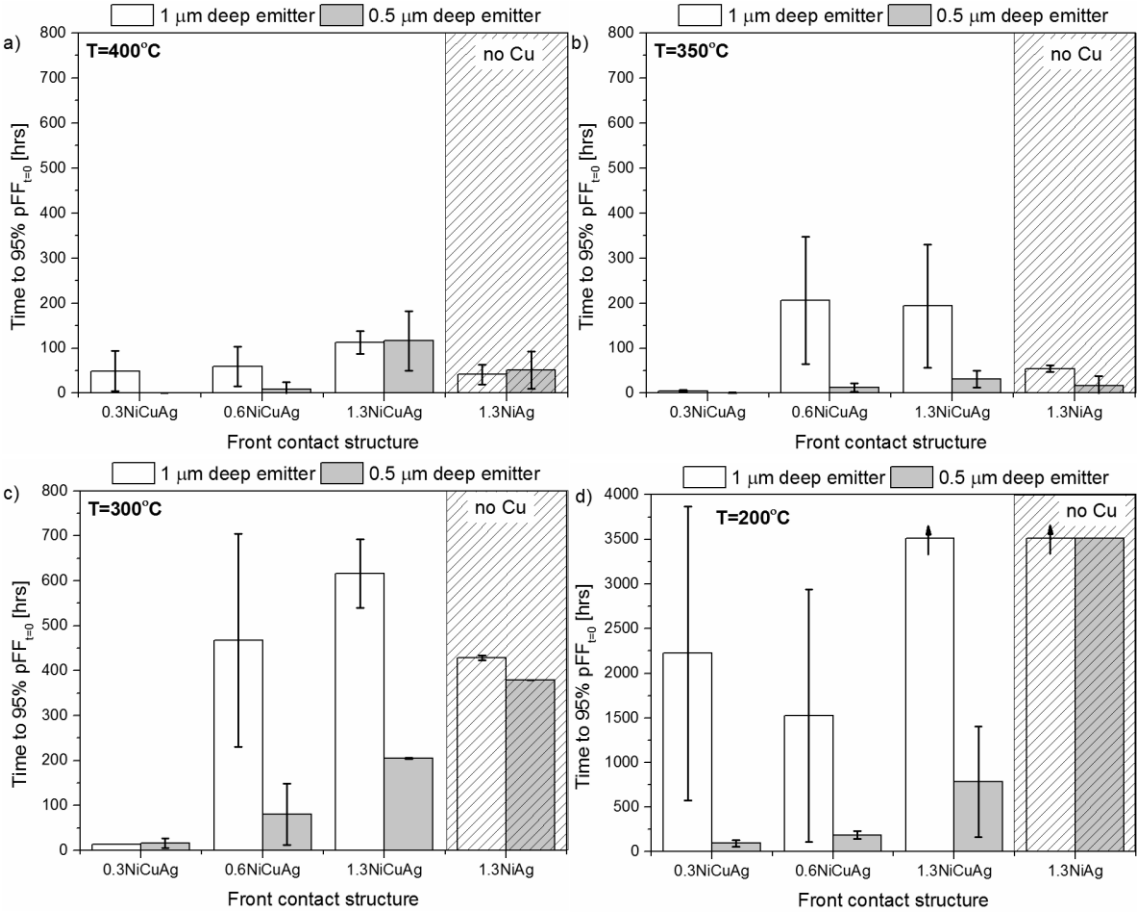


Figure 7.12: Time to failure (i.e. 95% of $pFF_{t=0}$) for various front contacts stacks and two different emitters depth after thermal stress at (a) 400˚C, (b) 400˚C, (c) 400˚C, and (d) 200˚C.

The fact that samples with only Ni/Ag failed, possibly due to Ni diffusion, indicates that both Ni and Cu diffusion could be happening concurrently in Ni/Cu/Ag samples. Nevertheless, Cu diffusion still appears to play a major as thin Ni barrier layers failed faster.

Cells with the 0.5 μm emitter failed faster than the 1 μm emitter which is unexpected as Cu diffusion in Si should be extremely fast thus failure independent of junction depth. Absolute pFF values were around 81.5% with the 0.5μm emitter, even before thermal ageing, as compared to >82% for the 1μm emitter (see Figure 7.11). The lower pFF can be understood by ps-UV laser ablation damage being more close to the junction. This damage might affect the kinetics of Ni or Cu diffusion. Thus it would be interested in the future to evaluate the effect of increasing ps-UV laser damage on the time to failure when keeping the junction depth constant. The fact that junction depth could influence time to failure has significant implications on the cell structure as devices with a deep junction under the contacts (e.g. laser doped selective emitter) or with the junction at the rear side could strongly benefit from this aspect. For this reason, implementation of Ni/Cu/Ag plated front contacts in a rear junction device is discussed in the next chapter.

Time to failure at operation conditions were estimated by fitting the data according to equation (7.3) as shown in Figure 7.13. Estimates for the 1μm with the reference Ni/Cu/Ag stack of 1.3/9/0.3 μm indicate that the cells would last ~200 years at 55˚C (~100 years at 85˚C) which provides evidence that long-term reliability is feasible. Also for this stack, we can show can these cells last much longer in the range of temperature tested than literature data currently available for similar cell structures. The estimated lifetime at operating conditions for samples without Cu is even longer (>>1000 years at 85 ˚C). Finally, it is important to observe that small uncertainties in the data can lead to important differences in estimated failure time at operating conditions. Similarly, the fact that having a device that fails relatively fast at low temperature and extremely fast at high temperature can lead to an extremely high failure time at operating conditions can be questionable. Therefore, the present accelerated thermal ageing results should be taken with caution and further tests are planned to build stronger confidence in these results.

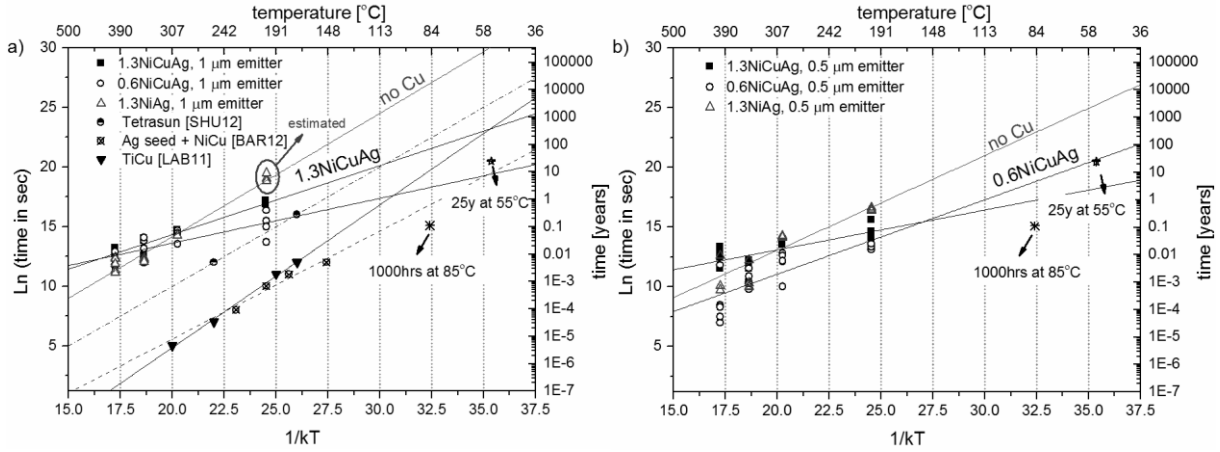


Figure 7.13: Arrhenius plots showing time to failure (i.e. 95% of $pFF_{t=0}$) as function of temperature for (a) 1 μm deep 120 Ω/sq emitter and (b) 0.5 μm deep 80 Ω/sq. Data taken from literature is also given in (a).

7.5. Chapter summary

The reliability of Ni/Cu plated contacts was addressed in this chapter as the generally observed poor mechanical stability of Ni/Cu as compared to conventional screen printed (SP) Ag contacts is seen a great source of concern in industry.

Adhesion between Ni/Cu plated contacts was first looked at in a sequence where sintering was performed directly after Ni deposition as this was the sequence of choice at the beginning of this thesis. Using this sequence, we could demonstrate excellent adhesion results provided that silicidation temperature was high enough and that unreacted Ni removal was followed by a short HF step. Poor adhesion results were linked to no/insufficient silicidation for the former and to the presence of an oxide-rich interface for the latter. We then could show the importance of ps-UV front laser ablation parameters and in particular that: (i) busbar opening fraction should be ~100%, (ii) pulse overlap/power must be optimized, (iii) pinning the finger extremities helps preventing finger delamination. Finally, moving the sintering step at the end and using an inline Ni/Cu/Ag plating machine we could maintain good adhesion results, meaning limited by wafer breakage, when using adequate Ni and Cu plating chemistries.

Following these results, we fabricated several Ni/Cu/Ag plated cells that were interconnected using either conductive adhesives or standard soldering. We could show that mini-modules and 10-cells strings modules with these cells passed both 1.5x thermal cycling and damp heat testing as defined in IEC61215. These results are particularly important as they give evidence that the adhesion results were relevant. Further environmental module testing is currently planned with full size 60-cells modules as this would help building confidence that mechanical stability of Ni/Cu plated contacts is not an issue.

Finally, tentative conclusions were made based on accelerated thermal ageing tests. Using the optimized Ni/Cu/Ag sequence developed in this thesis we estimated a failure time at 85˚C of ~100 years which provides evidence that long-term reliability is feasible. In addition, results obtained revealed that: (i) front dielectrics are not the weakest link to Cu diffusion, (ii) thick Ni barrier layers are preferred, and (iii) deep junctions are preferred. This last point has significant implications has it would mean that rear-junction devices with front Ni/Cu/Ag plated contacts could offer even greater long-term reliability. Moving the junction to the rear side also has other advantages that are presented in the next chapter.

CHAPTER 8

Towards rear junction n-PERT Si solar cells with fully plated contacts

In this chapter self-aligned Ni/Cu/Ag plated front contacts are applied to rear junction n-type devices since doing so potentially allows to sidestep several issues. These issues are reviewed in section 8.1 together with a literature review of rear junction n-type devices that led to the choice of a passivated emitter and rear totally diffused (PERT) cell design. Large area n-PERT results are presented in section 8.2. A power-loss analysis is conducted in section 8.3. and simulations that demonstrate the higher potential of n-PERT are presented in section 8.4.

8.1. Introduction

P-type silicon offers advantages that has made it the dominant material for terrestrial solar cell applications. Namely these are: (i) more uniform resistivity (typically ~3x variation across boron-doped CZ-Si ingots while it can be up to 10x with phosphorous-doped [GIA11]), (ii) lower processing temperatures for $POCl_3$ diffusion (as compared to BBr_3 diffusion) coupled with the ability to getter metal impurities, and (iii) process simplicity of Al-BSF solar cells with screen printed Ag (SP-Ag) front contacts (see Chapter 2.3.1). So far we have a developed a simple sequence to replace SP-Ag front contacts by Ni/Cu/Ag plated front contacts on front junction p-type devices. Though we could demonstrate efficiencies up to 20.7% on large area cells we have also shown that careful optimization was required to minimize junction damage (Chapters 5 and 6). In Chapter 6.2.2, we shortly addressed the fact that standard boron doped CZ-Si typically suffers from boron-oxygen related light-induced degradation (LID) and also the fact that common metal impurities (e.g. Fe) can lead to bulk lifetime degradation upon high temperature processing. In Chapter 7, we presented preliminary data indicating that deep emitters would be preferred to ensure long-term reliability. Considering these aspects and knowing that n-type material does not suffer from LID while it has a potential for higher diffusion lengths, it would make sense to evaluate Ni/Cu/Ag plated front contacts on rear junction n-type devices.

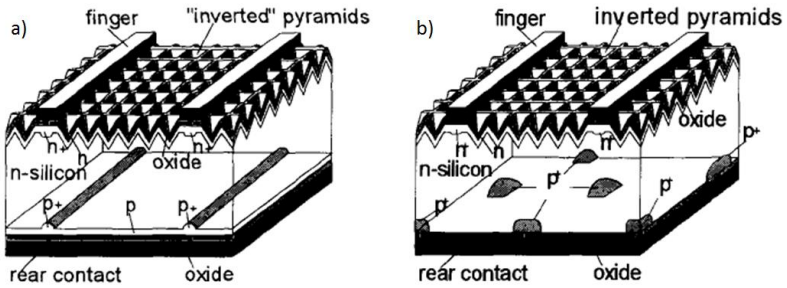


Figure 8.1 Passivated emitter rear totally- (PERT, (a)) and rear locally- (PERL, (b)) diffused solar cells. [DAI93].

Historically, rear junction n-type devices were first applied in interdigitated back contacts (IBC) solar cells with significant developments being made in the 1980s [GRA09]. More conventional passivated emitter rear totally- (PERT) and rear locally- (PERL) diffused n-type cell structures with contacts on both sides (see Figure 8.1) were introduced in 1993 by Dai et al. [DAI93]. For the former, results have been mostly reported using boron diffusion or aluminum alloying to form the rear p^+ emitter. Using boron diffusion, Zhao et al. [ZHA06] reported efficiencies up to 22.7% on small area (22 cm^2) FZ-Si. More recently, Mertens et al. [MER13] reported efficiencies up to 21.3% on large area (243 cm^2) using SP-Ag front contacts. For screen printed Al-p^+ rear junction on large area (238 cm^2), Schmiga et al. [SCH10] reported an efficiency of 19.3% for cells with an unpassivated rear and 20.0% for cells where the rear side Al-p^+ emitter was passivated by Al_2O_3/SiN_x. Applying self-aligned Ni/Cu plated contacts to front junction p-type Al-BSF solar cells (i.e. n^+pp^+ structure) or to Al-p^+ rear junction n-type cells (i.e. n^+np^+ structure), Rauer al. [RAU13b] could confirm that rear junction n-type cells are much less sensitive to damage created during nickel silicide formation. Efficiencies up to 22.3% on large area (243 cm^2) CZ-Si have also been demonstrated by CIC Choshu using a heterojunction (i.e. amorphous Si layers on both sides of CZ-Si substrate) rear emitter cell structure [KOB13]. However, high efficiencies obtained in heterojunction devices are the result of reduced recombination under the metal contacts because they are electronically separated from the substrate [DeW12]. Therefore, our sequence to define Ni/Cu/Ag plated contacts in direct contact with Si is not compatible with such devices. In fact, high efficiency heterojunction cells featuring Cu plated contacts have mostly been obtained with a more complex masking approach (see Chapter 3.2.5). This leaves us the choice between n-type rear junction PERT or PERL devices.

Considering that rear junction PERL cell structures are more prone to current crowding issues at the local rear p^+ areas [DAI93] and to shunting issues due to the rear p^+ metal contacting the n-type base [DAI93, SCH10], we opted for a n-type rear junction PERT cell structure. BBr_3 boron diffusion was chosen to form the blanket rear p^+ emitter in this cell structure that we will name n-PERT in the rest of this chapter. On top of tackling issues mentioned above with front junction devices, the chosen n-PERT structure presents additional advantages. First, the Ni/Cu/Ag plating sequence that includes bias-assisted LIP Ni/Cu steps can be identical to the one developed on front junction p-type devices since plating still occurs on the n^+ side. Bias-assisted LIP on front junction n-type devices (i.e. plating on p^+) is more challenging because the p^+ side is always on a more positive potential (see Chapter 5.4.2). In cases where the cell is fully immersed in the electrolyte, bias-assisted LIP would result in preferential plating at the rear n^+ side rather than at the front p^+ side. As discussed by Mette [MET07], plating only at the front p^+ side is possible by keeping the backside dry (or masked) and operating the cell in forward bias in the dark. But, again, having Ni/Cu/Ag contacts close to the *pn* junction increases risks of junction damage due to front patterning/metallization process. Second, the blanket rear p^+ emitter eliminates the high bulk spreading resistance (see Chapter 6.1). Finally, since the Al rear contact does not need to be fired, n-PERT cells should have improved rear reflectance compared to p-type i-PERC cells with rear Al firing (see Chapter 6.2.6).

8.2. Proof-of-concept

The respective process sequence for p-type i-PERC and n-PERT silicon solar cells with Ni/Cu/Ag plated front contacts are shown in Figure 8.2. The resulting cell structures are given in Figure 8.3. To evaluate the potential of both cell structures extensive cleaning steps are present before all high temperature (>800˚C) processing. Apart from extra cleaning steps, the n-PERT sequence adds three extra steps while eliminating two others compared to the p-type i-PERC sequence. These three extra steps are: (i) saw damage removal, (ii) BBr_3 diffusion, and (iii) thermal oxidation to drive-in the p^+ emitter and form a relatively thick (~200 nm) thermal oxide. Following this, the thermal oxide is selectively removed at the front side in HF which enables subsequent random pyramid texturing. Such an approach introduces external gettering (i.e. impurities gettered in front p^+ are etched away) and eliminates the rear inline polishing step used with p-type i-PERC since wafers are textured only on one side. In addition, the rear inline emitter removal step is no longer needed since the thick thermal oxide at the rear is used as a mask during $POCl_3$ diffusion. For both cell structures the remaining front side processing steps are identical: (i) $POCl_3$ diffusion, (ii) thermal oxidation to drive-in dopants forming a ~1 µm deep homogeneous n^+ at the front as well as a high quality SiO_2 passivation, (iii) plasma enhanced chemical vapor deposition (PECVD) of SiN_x, (iv) front ps-UV laser ablation, (v) Ni/Cu/Ag plating in the MECO tool and (vi) silicidation in a belt furnace under nitrogen (N_2).

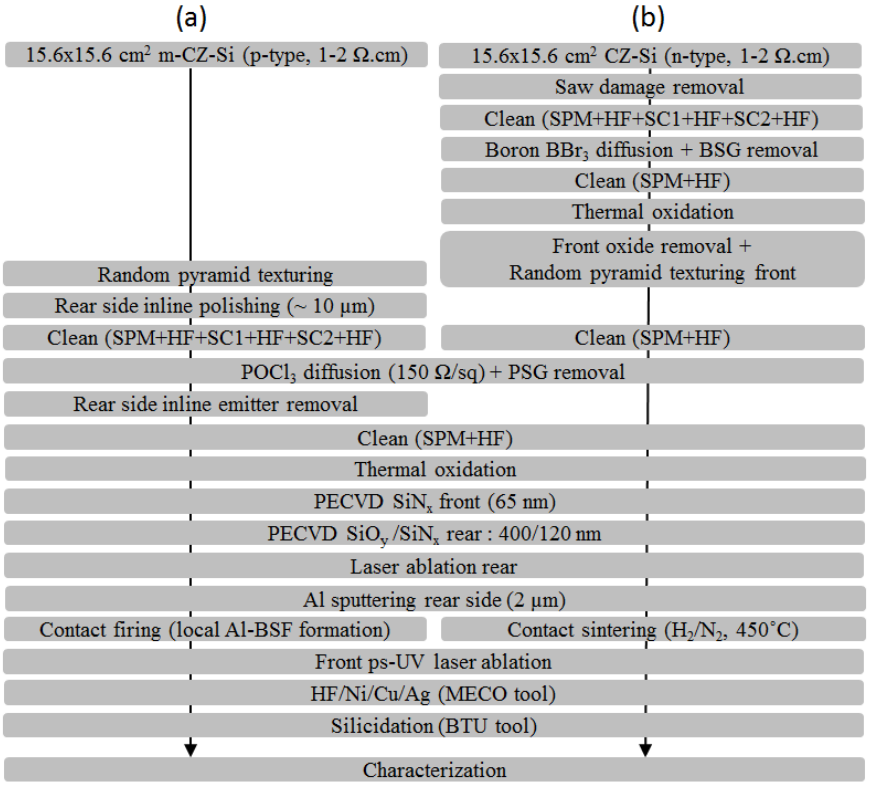


Figure 8.2 Process sequence for: (a) p-type i-PERC and (b) n-type PERT.

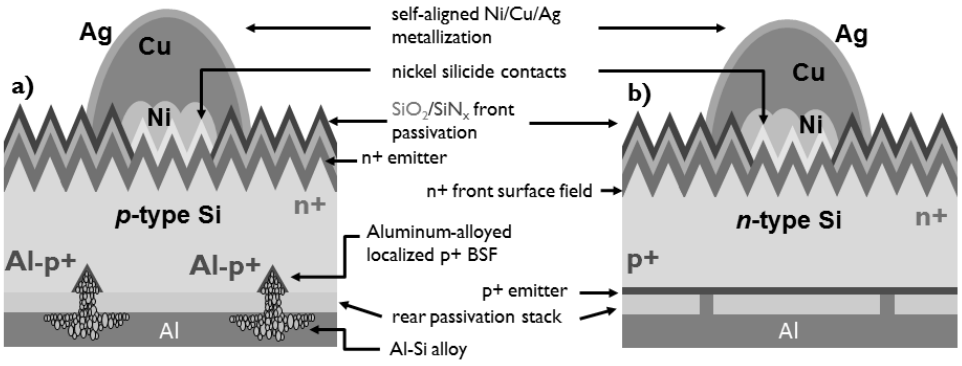


Figure 8.3 Cell structure schematic for : (a) p-type i-PERC and (b) n-type PERT.

By implementing the changes mentioned earlier, we were able to produce n-PERT solar cells on 156 mm with top efficiencies of 20.5% (see Table 8.1) and encouraging open-circuit voltage values (V_{oc}~674±2mV) as compared to p-type i-PERC (V_{oc}~656±5mV). It should be mentioned that 156mm p-type i-PERC suffered from areas within the cells with poorer bulk lifetime explaining the larger spread in open-circuit values and efficiencies. Despite the fact than a wider front contact spacing (1.5 mm for n-PERT, 1 mm for p-type i-PERC) was chosen to minimize front grid shading, n-PERT cells lead to short-circuit current density values ~1 mA/cm^2 lower. This is because in rear junction cells, minority carriers, mostly generated near the top surface by short wavelength photons need to diffuse a long distance before reaching the rear *pn* junction where they can be collected [DAI93]. Therefore, further reduction in front surface recombination should greatly improve short-circuit current density values and hence efficiencies of n-PERT devices. This point is addressed in next sections. Though pFF values were comparatively lower on n-PERT in this experiment, we could demonstrate pFF values up to 83.5% by optimizing rear laser ablation in subsequent experiments. This shows that moving the junction to the planar rear side is the correct strategy to improve efficiencies which is not surprising since damage-free laser ablation is much easier to obtain on flat surfaces [HER10b].

Table 8.1: Average (4 cells) and best cell electrical results for 156mm p-type i-PERC and n-PERT cells after sintering of the Ni/Cu/Ag contacts. Series resistance and busbar-to-busbar resistance (R_{bb}) are given as indication.

Device	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	ŋ [%]	r_s [Ω.cm^2]	n	pFF [%]	R_{bb} [mΩ]
i-PERC average	38.8 ± 0.2	655.9 ± 4.6	79.5 ± 0.7	20.2 ± 0.4	0.64 ± 0.17	1.06 ± 0.02	83.1 ± 0.2	18.7 ± 7.2
i-PERC best	39.0	661.0	80.0	20.6	0.53	1.07	83.0	14.8
n-PERT average	37.9 ± 0.4	674.0 ±2	80.1 ± 0.7	20.4 ± 0.1	0.51 ± 0.15	1.12 ± 0.02	82.7 ± 0.3	19.0 ± 4.9
n-PERT best	38.4	675.9	79.2	20.5*	0.64	1.13	82.6	24.6

*Externally confirmed at FhG-ISE CalLab

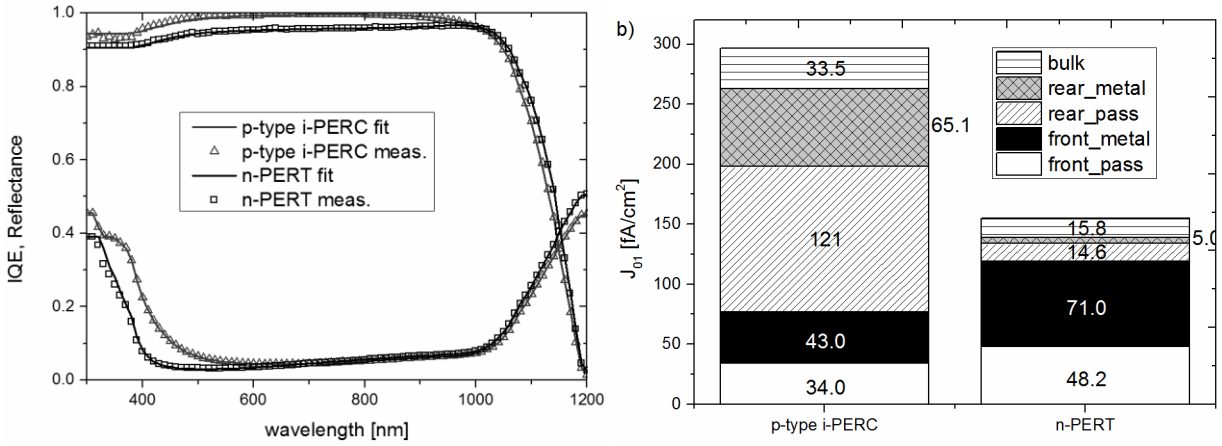


Figure 8.4 a) Internal quantum efficiency (IQE) and reflectance curves (measured and PC1D fit) for the best p-type i-PERC and n-type PERT cells in Table 8.1. b) Breakdown of j_{01} recombination for p-type i-PERC and n-PERT.

The higher sensitivity of n-PERT cells to front surface recombination was confirmed from spectral response measurements since measured internal quantum efficiency values are much lower for wavelengths up to 1000nm than with the best p-type i-PERC (see Figure 8.4a). Extracting the light trapping parameters from the linear fit of 1/IQE versus the absorption depth (1/α) (see Chapter 6.1), we find an internal rear reflectance ~92% which is comparable to the one of the best p-type i-PERC cell which is unexpected. As shown in Chapter 6.2.6 for an identical $SiO_2/SiO_y/SiN_x$/Al rear stack, not firing the rear Al as done in n-PERT devices should reduce parasitic absorption of long wavelengths in the rear Al thereby increasing internal rear reflectance. However, free carrier absorption (see Chapter 2) in the front n^+ and the additional p^+ blanket rear emitter present in n-PERT could also limit visible improvements in internal rear reflectance. Further optimization of the rear emitter and rear dielectric stack should provide a clearer picture of the exact internal rear reflectance losses in n-PERT devices

As discussed in Chapter 6.1, individual dark saturation current density (j_0) contributions were obtained from QSSPC-PL measurements on co-processed test wafers. The ~20 mV gain in V_{oc} with n-PERT compared to p-type i-PERC is mainly the result of drastic reductions in rear dark current saturation densities as shown in Figure 8.4b. Excellent $j_{0,rear,pass}$ ~15 fA/cm^2 were measured for the rear p^+ emitter as opposed to $j_{0,rear,pass}$ ~120 fA/cm^2 extracted on p-type i-PERC. Recombination at the rear side contacts is also lower in n-PERT because of the reduced contact fraction (~0.3% as compared to ~2.1% used for these p-type i-PERC). Interestingly, we extracted much higher $j_{0,front,metal}$ (71 fA/cm^2) for n-PERT than with the p-type i-PERC cells (43 fA/cm^2) despite the wider front grid design (1.5mm versus 1mm). N-PERT cells also suffered from higher $j_{0,front,pass}$ which can be explained by the absence of emitter removal step leading to sheet resistance for the front n^+ around 100Ω/sq (120Ω/sq for p-type i-PERC) and hence to $j_{0,front,pass}$~50fA/cm^2 (35 fA/cm^2 for p-type i-PERC). These last two points demonstrate that the present n-PERT design offers a lot to further improve open-circuit voltage values and hence has potential for higher cell efficiencies than p-type i-PERC cells.

8.3. Power loss analysis

We performed a power-loss analysis of the best p-type i-PERC and n-PERT cells. Internal rear reflectance losses (see Figure 8.5a) are comparable (~0.45 mW/cm^2). The n-PERT cell benefits from reduced front reflectance losses (1.7 mW/cm^2 versus 2.2mW/cm^2) because of reduced grid shading and reduced reflectance at short wavelengths. As expected, resistive losses in the bulk of n-PERT cells are reduced by a factor 10 as compared to p-type i-PERC cells (see Figure 8.5b). Unsurprisingly, resistive losses at the front side (front finger, contact resistance to n^+, and front n^+) are higher in n-PERT than in p-type i-PERC due to the wider grid spacing that was adopted. Finally, the fact that resistive losses in the rear p+ emitter of n-PERT cells only account for 0.1mW/cm^2 (out of 0.86 mW/cm^2) shows that the rear contact pitch is appropriate.

Summarizing the different power loss contributions (see Figure 8.6), we find that n-PERT offers: reduced recombination losses at V_{oc}, lower (front) reflectance losses, and slightly higher FF losses. However, the present n-PERT design suffers from higher recombination losses at j_{sc}.

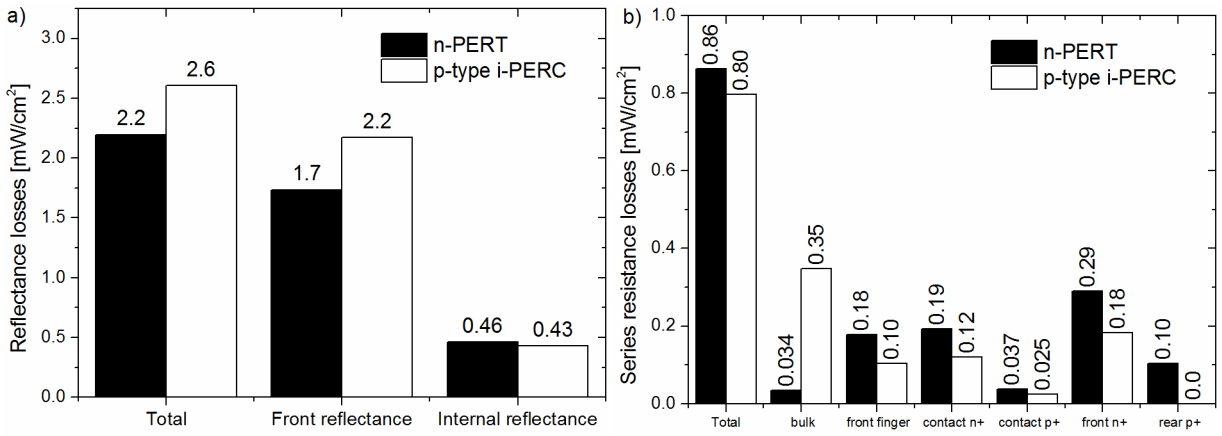


Figure 8.5 Breakdown of (a) reflectance losses and (b) series resistance losses for n-PERT and p-type i-PERC.

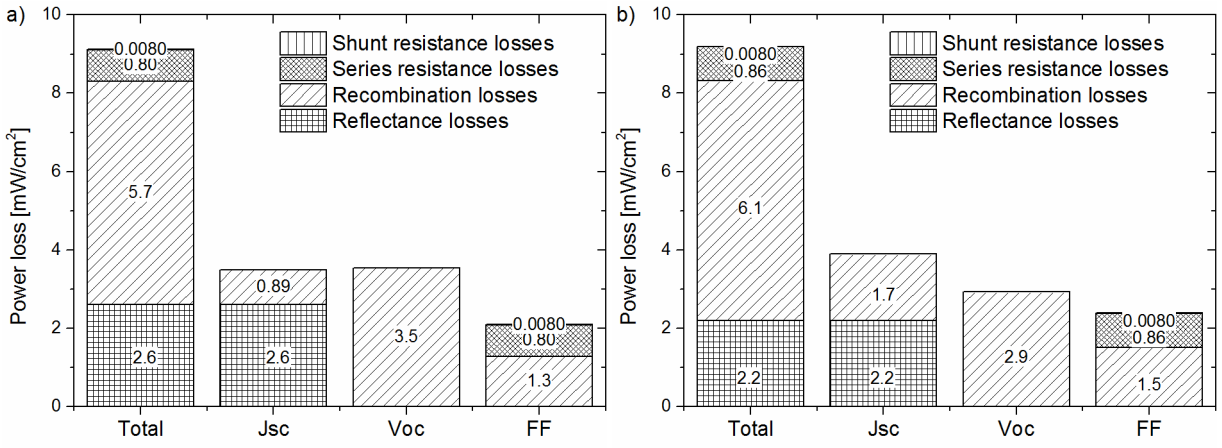


Figure 8.6 Total power loss breakdown for (a) p-type i-PERC and (b) n-PERT.

8.4. Future improvements

In this section, PC1D simulations were performed on the basis of the best 156 mm p-type i-PERC and best 156 mm n-PERT device parameters given in Table 8.2. The front surface recombination velocity (SRV) is higher in n-PERT than on p-type i-PERC while the rear SRV is much lower due to the excellent J_0 of the rear blanket p^+ emitter. As mentioned before, p-type i-PERC cells suffered from lower bulk lifetime while n-PERT cells gave lower pFF values. The lower pFF values are reflected by the slightly higher internal diode current density (j_{02}). Overall, simulated PC1D J-V results are in good accordance with measured values.

Table 8.1: Average (4 cells) and best cell electrical results for 156mm p-type i-PERC and n-PERT cells

Description	unit	p-type i-PERC	n-PERT
Front + rear series resistance	[Ω.cm^2]	0.5	0.6
Front SRV	[cm/s]	5100	5250
Rear SRV	[cm/s]	110	15
Resistivity	[Ω.cm]	2	1.65
Bulk lifetime	[µs]	1080	1500
Internal diode j_{02} (n=2)	[A/cm^2]	7.0x10^{-09}	9.3x10^{-09}
PC1D simulated j_{sc}	[mA/cm^2]	39.0	38.4
PC1D simulated V_{oc}	[mV]	660.9	675.9
PC1D simulated FF	[%]	79.9	79.2
PC1D simulated Efficiency	[%]	20.6	20.5

We first estimated the impact of reducing recombination at the front surface as this was shown to have a significant impact on cell results obtained. Reducing the front SRV from the current 5100 cm/s down to 1000 cm/s we estimate a further 0.4%$_{abs.}$ increase in efficiency for p-type i-PERC cells (see Figure 8.7a). Such a low front SRV value has already been reported for laser doped selective emitter (LDSE) which is a technology already implemented in production [WAN12]. Implementing such a technology in n-PERT would lead to a selective front surface field (FSF). Comparatively, reducing the front SRV from the current 5250 cm/s down to 1000 cm/s on n-PERT would provide a 1%$_{abs.}$ gain in efficiency leading to energy conversion efficiencies above 21.5%. Further efficiency gains could be expected as the impact on contact resistance and pFF of heavy doping under the front contacts was not taken into consideration.

In addition, n-PERT cells present higher tolerance to thinner wafers as shown in Figure 8.7b. Reducing wafer thickness down to 100 µm, would result in a slight efficiency gain (~0.1% abs.) for the current high SRV values. This has significant implications as despite extremely low poly-Si prices, standard 180 µm wafers account for 40 to 60% of total cell manufacturing costs which could be strongly reduced by moving to 80 µm thick [GOO13].

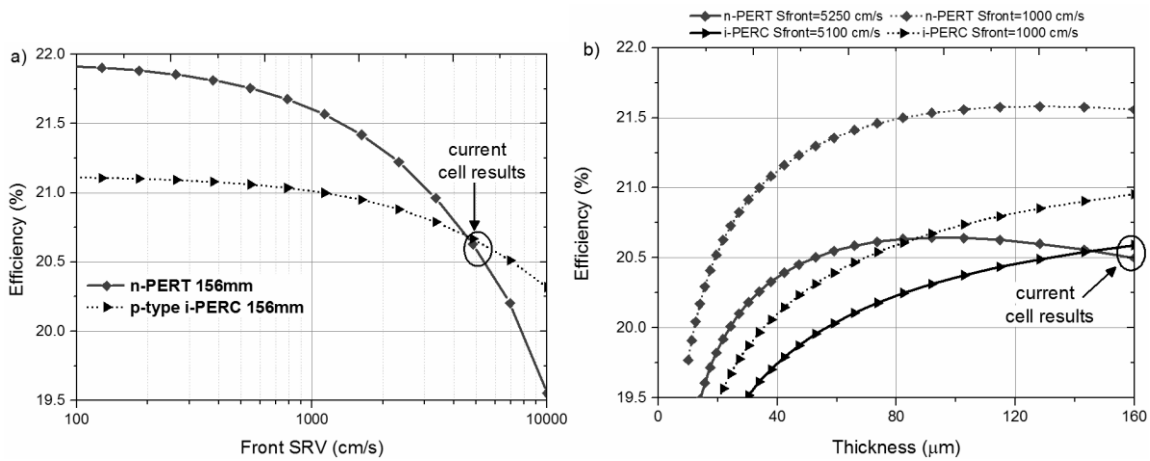


Figure 8.7 a) PC1D simulated efficiency for p-type i-PERC and n-PERT cells for varying front surface recombination velocities (SRV). b) PC1D simulated efficiencies for p-type i-PERC and n-PERT cells for varying wafer thicknesses and for two different front SRV values.

Finally, we simulated the impact of varying bulk resistivity since less uniform resistivity across the ingot is seen as a disadvantage for n-type material. In a first approximation we assumed bulk lifetime τ_{bulk} to be limited by solar cell processing steps. Constant τ_{bulk} of 1.5ms and 0.2ms were assumed for n-PERT and p-type i-PERC respectively. The 0.2ms τ_{bulk} on p-type was used to fit experimental results obtained on gallium doped p-type i-PERC cells [HOR12]. For this case, the rear series resistance component in PC1D was varied as a function of bulk resistivity to account for spreading resistance in the bulk. The corresponding variation in spreading resistance that was considered is in the range of 0.02 to 0.34 $\Omega.cm^2$ for a bulk resistivity varying from 0.2 to 3 Ω.cm. As seen in Figure 8.8, using the current front SRV values Ga-doped p-type i-PERC cells benefit from lower resistivity material thanks to increased V_{oc} and reduced spreading resistance. On the other hand, higher resistivity material would be preferable on n-PERT which is in accordance with earlier investigations [BAL13]. In particular, higher j_{sc} values would be obtained as the n^+ FSF becomes more effective with increasing bulk resistivity. Finally, for front SRV=1000 cm/s, n-PERT cells would become tolerant to a wide range of resistivity values with efficiencies around 21.5% for bulk resistivity ~2-10 Ω.cm.

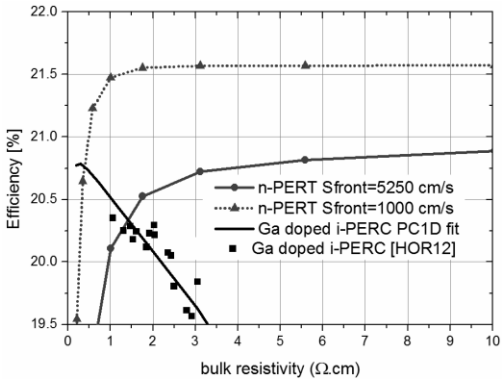


Figure 8.8 PC1D simulated efficiencies for p-type i-PERC and n-PERT for varying bulk resistivity.

8.5. Chapter summary

In this chapter self-aligned Ni/Cu/Ag plated front contacts were applied to rear junction n-type devices since doing so potentially allows to sidestep several issues encountered when applying the same contacts to front junction p-type devices. A passivated emitter and rear totally diffused (PERT) cell design was chosen based on literature review. By making a few modifications to the p-type i-PERC sequence optimized in Chapter 5 and 6, we were able to fabricate in a first trial large area n-PERT cells leading to efficiencies up to 20.5% and encouraging open-circuit voltage values (V_{oc}~674±2mV) as compared to p-type i-PERC (V_{oc}~656±5mV). Excellent $J_{0,rear,pass}$ ~15 fA/cm^2 were demonstrated for the BBr_3 diffused rear p^+ emitter passivated by a thick thermal oxide. Other J_0 results indicated that there is a lot of room to further improve open-circuit voltage values in n-PERT devices.

A power-loss analysis was conducted which led to the conclusions that the present n-PERT design offers: reduced recombination losses at V_{oc}, lower (front) reflectance losses, and slightly higher FF losses than the standard p-type i-PERC design. However, we also found that this design is extremely sensitive to front recombination, in particular under the front contacts.

Future process improvements were then estimated on the basis of PC1D simulations. Reducing the front surface recombination velocity (SRV) down to 1000 cm/s, efficiencies up to 21.5% were calculated for n-PERT cells as compared to 21% with p-type i-PERC cells. Simulations also revealed that reducing wafer thickness down to 80-120µm had a positive impact for n-PERT cells thus enabling a reduction in wafer costs. Finally, the n-PERT design was shown to be potentially tolerant to a wide range of bulk resistivity thereby indicating that a very large portion of n-type CZ ingots can be used unlike originally foreseen.

Overall, the work presented in this chapter demonstrates the higher efficiency potential of rear junction n-PERT devices with Ni/Cu/Ag plated front contacts as compared to front junction p-type i-PERC devices with Ni/Cu/Ag plated front contacts. Solutions (selective FSF, improved rear ablation, thinner wafers, etc.) to tackle the main losses in n-PERT were suggested which should enable efficiencies beyond 21% on large area in the near future. However, improved long-term reliability and larger process window for the definition of the Ni/Cu/Ag plated front contacts, as compared to p-type i-PERC, have yet to be demonstrated with n-PERT. Investigations that apply the methodology described in Chapter 6 and 7 are currently being started at imec to address these two aspects. Such investigation should also demonstrate that the higher sensitivity of n-type material to copper [MAC07] is not an issue for long-term reliability.

CHAPTER 9

Excimer laser annealing as an alternative to rapid thermal annealing

In this chapter, we present an alternative nickel silicidation method to conventional rapid thermal annealing (RTA) named excimer laser annealing (ELA). First, we use p-type PERC solar cells and demonstrate that it is possible to irradiate the entire front side to form self-aligned nickel silicide contacts by ELA without damaging significantly the surrounding dielectric(s). Second, a hybrid n-PERT cell design is proposed and we show that ELA of the front contact is compatible, unlike RTA, with blanket amorphous Si layers as rear passivation.

9.1. Motivation

One challenge with the integration of nickel silicide contacts is to control nickel silicide formation as to obtain to desired phase without degrading device performance. Metrics for device performance are junction leakage (measured in reserved bias) in IC industry and j_{02} recombination (measured in forward bias) for solar cell devices, both of which should be kept as low as possible. In chapter 5.2 we demonstrated that j_{02} recombination could be reduced by lowering the sintering temperature to form the more resistive phase Ni_2Si and by using deeper junctions. In IC industry where the less resistive NiSi phase is required and deeper junction are not an option, two low temperature rapid thermal annealing (RTA) steps are usually applied with a selective unreacted Ni etch inserted between the two anneals. The trend in recent years has been to lower thermal budget by heating to higher temperatures for brief periods since this was shown to reduce Ni diffusion/agglomeration and contact resistance. Results have been published replacing the second RTA by: spike anneal [LAU04, ADA07], millisecond (ms) anneal (MSA) [CHE09, HEB11, ADA07], or laser thermal annealing (LTA) [BAR96, LEE06, SET06].

Though lasers may be used for MSA, there are differences with LTA. Laser-based MSA is typically performed by scanning a continuous wave infra-red laser across the surface leading to complete wafer heating by free carrier absorption [HEB11]. This results in temperatures in the range of 500-1000˚C for a few ms and hence nickel formation by solid-state diffusion as with conventional RTA. LTA typically uses ultra-short (<1 μs) excimer UV-laser pulses leading to absorption of laser-light in the near-surface region [VEN12, HUE12]. This enables excellent control of nickel silicide formation in either in the melt regime or in the non-melt regime when associated with a previous RTA step [BAR96, LEE06, SET06]. Thus, LTA seems an interesting alternative to RTA for the definition of front nickel silicide contacts in solar cells since it may enable: (i) improved control of nickel silicide phase formation, (ii) reduced j_{02} recombination on shallow emitter devices, and (iii) passivation schemes at the rear side that cannot withstand RTA.

Excimer lasers are lasers that are electrically pumped using a high-voltage discharge. Excimer gas media commonly consist of an inert gas such as argon (Ar), krypton (Kr) or xenon (Xe), and a reactive gas such as fluorine (F_2) or chlorine (Cl). Excimer lasers take their name from the "excited dimers" that form when the gas mixture is electrically excited, and emit UV light. Most common excimer lasers are F_2 (157nm), ArF (193nm), KrF (248nm), and XeCl (308nm) which are used for applications ranging from photolithography to eye surgery [BAS05].

Experiments in this chapter were performed using a XeCl laser from EXCICO (LTA series) which is already in production for several applications in IC industry [VEN12]. This laser can deliver a high energy per pulse (up to 15 J) which enables to irradiate several square millimetres in a single pulse (up to 18x18mm^2 in this work). It features a top-hat profile (±2 % power uniformity within the pulse area) with a long pulse duration (~180 ns) which was shown to enable improved control of melting depth and defect generation [HER03, VEN04, HUE09]. For simplicity, tests performed using EXCICO's laser are referred to as excimer laser annealing (ELA) and nickel silicide formation by ELA was evaluated as direct replacement to RTA.

9.2. Excimer laser annealing (ELA) in front junction p-type i-PERC cells

9.2.1. Nickel silicide formation by ELA

To demonstrate nickel silicide formation by ELA we used a thin (40 nm) Ni layer that was sputtered on various p-type CZ-Si substrates. A fluence map was performed on each substrate type by shooting single 1 cm^2 ELA pulses with fluence values in the range of 0.5 to 2 J/cm^2. Unreacted Ni was removed in a H_2SO_4:H_2O_2 (5:1) mixture. Nickel silicide formation was evaluated by performing 4 point probe sheet resistance (R_{sh}) measurements in each laser shot.

In Figure 9.1a, R_{sh} results are compared for two substrate types: 725 µm thick mirror polished (ρ=12-24 Ω.cm, R_{sh} >165 Ω/sq) and 160 µm thick random pyramid textured (ρ=2-3 Ω.cm, R_{sh} >125 Ω/sq). We observe a sharp drop in R_{sh} values for increasing fluence values up to 1 J/cm^2 followed by a slow increase in R_{sh}. Nickel silicides are formed on textured samples at fluence as low as 0.5 J/cm^2 while at least 0.7 J/cm^2 are required on mirror polished samples.

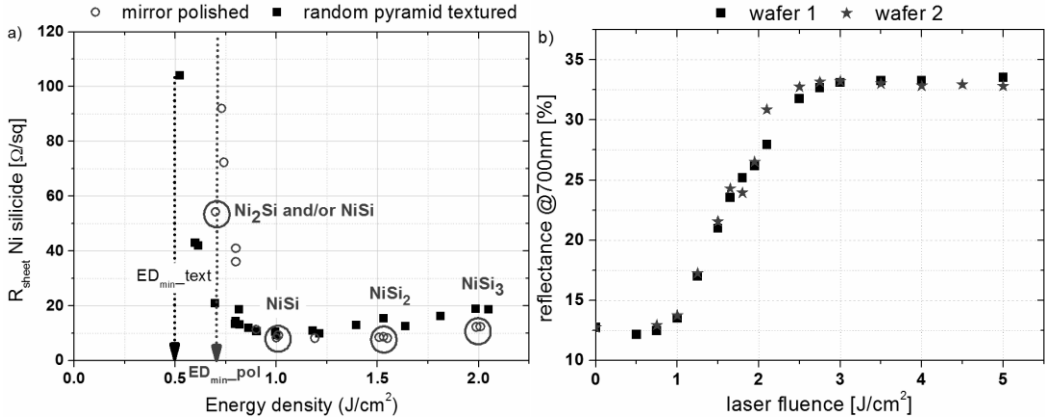


Figure 9.1 a) Sheet resistance (R_{sh}) of nickel silicides formed vs. excimer laser fluence for 725-µm thick mirror polished (○) and 160-µm thick random pyramid textured (■). Silicide phase composition as extracted from Rutherford backscattering (RBS) is indicated. b) reflectance vs. laser fluence on alkaline textured samples (no Ni).

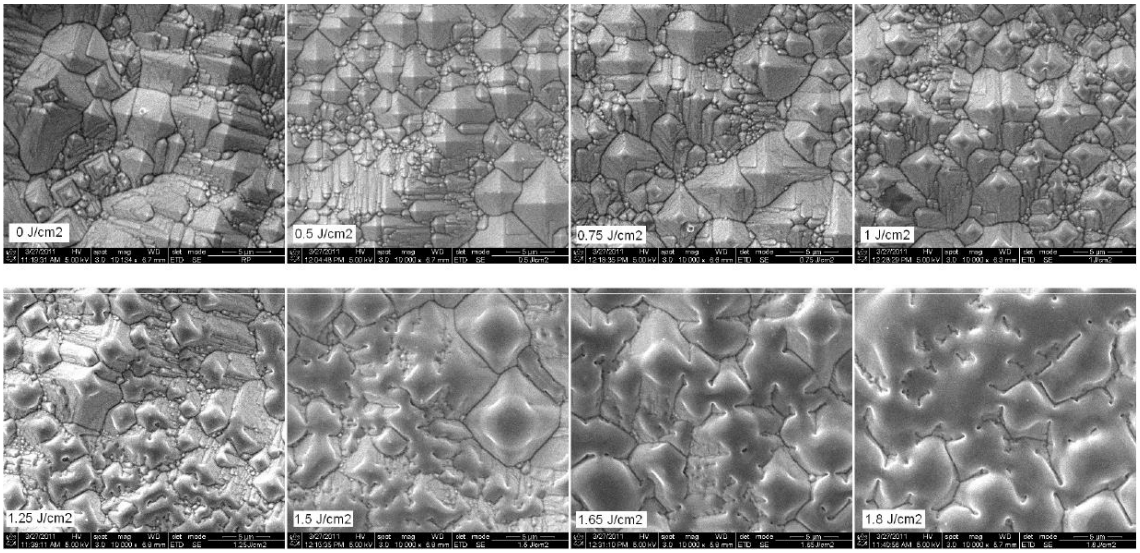


Figure 9.2 From left to right and from top to bottom: scanning electron microscopy images of alkaline textured samples after being irradiated by increasing excimer laser fluence values.

Rutherford backscattering measurements (RBS) were performed on mirror polished samples to determine phase composition. RBS results indicate direct formation of the low resistive NiSi phase at fluence values around 1 J/cm^2 followed by the formation of the more resistive $NiSi_2$ phase above 1.5 J/cm² thereby explaining the slow increase in R_{sh} at higher fluence values. At 0.7 J/cm^2, the layer created was too thin to accurately determine by RBS if Ni_2Si and/or NiSi were present. The sharp drop in R_{sh} values above 0.7 J/cm^2 could reflect either a change in silicide composition and/or a rapid increase in silicide thickness. Silicide formation occurred much below the threshold for Si melting on planar surface (~1.6 J/cm^2). This indicates that silicide formation could occur in the non-melt regime or that the presence of Ni could help melting Si at low fluence values. Simulations are presented below that clarify these points.

The lower threshold on textured samples is the result of higher absorbance at 308 nm (not shown) and the fact that pyramid tips both receive more light due to light-trapping (see Chapter 5.1) and dissipate heat slower. Fluence maps performed on alkaline textured samples without any Ni at the surface indicated that reflectance increased above 0.75 J/cm^2 (see Figure 9.1b) due to Si melting in the pyramid tips causing them to round as shown in Figure 9.2. Therefore, nickel silicides formed on alkaline textured surface might not be continuous at fluence values around 0.5 J/cm^2 since only the very top of the pyramids tips melted at such low fluence values.

Transmission electron microscopy (TEM) and high-angle annular dark field scanning electron microscopy (HAADF-STEM) pictures were taken after selective unreacted Ni removal on pyramid textured samples to check the silicide composition and thickness uniformity along the pyramid edges and tip. The silicide composition was evaluated by energy dispersive X-ray spectroscopy (EDS). EDS line scans were performed perpendicularly to the <111> pyramid facets (e.g. going from NiSi into Si) which allows for sub-nm lateral resolution thanks to the thin TEM lamella (<100 nm). In Figure 9.3, HAADF-STEM images after ELA at 0.5 J/cm^2 or at 0.9 J/cm^2 are compared with nickel silicides formed by RTA at 250°C for 150 s or at 350°C for 30 s.

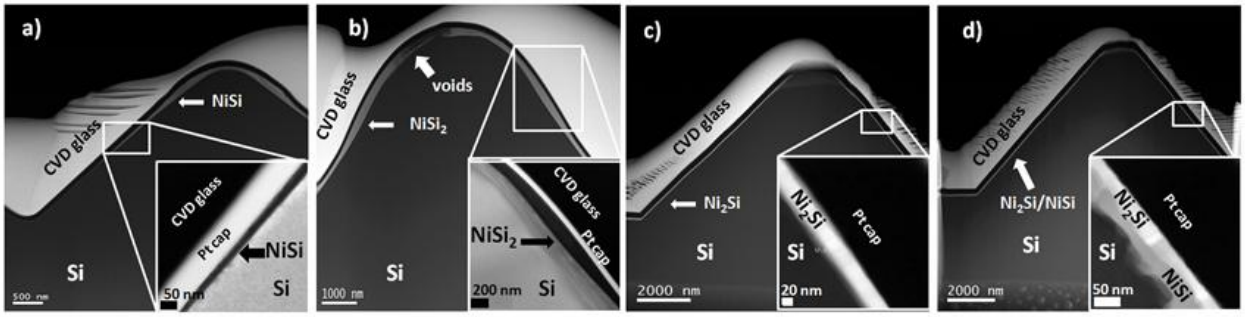


Figure 9.3 High angle annular dark field scanning transmission electron microscopy (HAADF-STEM) pictures on random pyramid textured Si(100) after (a) excimer laser annealing at 0.55 J/cm^2 (b) at 0.9 J/cm^2 (c) rapid thermal annealing (RTA) at 275˚C for 150 s and (d) RTA at 350˚C for 30 s. In HAADF-STEM mode, the contrast is proportional to Z^2 with Z the atomic number, and hence, heavier elements are visualized brighter than the lighter ones. The inserts in Figure 2(a) and (b) are taken in TEM mode, and hence, the bright/black contrast is reversed compared with the ones in Figure 2(c) and (d), which are taken in HAADF-STEM mode.

Direct formation of NiSi in a single ELA shot is observed in TEM images at fluence values as low as 0.55 J/cm^2 (see Figure 9.3a) supporting the previous R_{sh} results. The silicide thickness is larger at the pyramid tip (>100nm while it is <50nm in the valley). From Figure 9.3b, It is also evident that 0.9 J/cm^2 leads to higher Si consumption and hence $NiSi_2$ formation as already observed from RBS measurements. Voids are locally present at the pyramid tip which may contribute to the measured R_{sh} increase at high fluence values. In both cases, Si interfacial roughness is relatively low and continuous nickel silicide are observed along the pyramid edges.

On the contrary and as presented in Chapter 5.2, conventional RTA at 350˚C leads to rapid conversion of the Ni_2Si phase into NiSi (Figure 9.3d). This results in high Si interfacial roughness, due to non-uniform Ni diffusion, which has been linked to junction leakage in IC devices (see introduction). Lowering RTA temperature leads to reduced interfacial roughness but with the consequence that only Ni_2Si is formed (Figure 9.3c). Therefore, ELA seems to be a more attractive option since it is shown to enable direct formation of the low resistive NiSi phase while minimizing interfacial roughness.

9.2.2. Impact of Ni thickness

To understand nickel silicide formation by ELA and the observed NiSi formation at fluence as low at 0.7 J/cm^2 on flat substrates, simulations were performed using a finite element model. This model applies the phase-field methodology particularized to the excimer laser used in our experiments. Material, thermal, and optical parameters used in these simulations are given in Table 9.1. Detailed equations can be found in a joint publication with EXCICO [TOU13].

In Figure 9.4a, we compare simulated Si melting depth versus ELA fluence for various PVD Ni thicknesses. The increase in Si melting depth is modest (<1nm.mJ^{-1}.cm^{-2}) because of the small absorption depth in Si (α<10 nm) of the ELA laser (λ=308 nm) and its short pulse duration (~180 ns) enabling temperature ramp-down rates up to 10^3 ºC/s which are orders of magnitudes higher than with RTA [VEN12]. Thus, ELA enables excellent nickel silicide thickness control.

Table 9.1: Thermal (conductivity K, specific heat capacity c_p), material (density ρ, melting point T_m), and optical (refractive index n and extinction coefficient k) parameters used in the simulations of the ELA process. [TOU13].

Parameter	Value or expression (Refs. 12, 13)				Units
	Si_solid	Si_liquid	Ni	SiN_x	
$K_{T\leq1200K}$	$1523.7(T)^{-1.226}$	$0.502+2.93\times10^{-4}\,(T-T_c)$	0.907	-	[W/cm/K]
$K_{T>1200K}$	$9(T)^{-0.502}$			-	[W/cm/K]
c_p	$10\times T^{(1.034)/(1.02+0.01*T)-213}$	1045	444	17	[J/kg/K]
ρ	2320	2520	8900	3100	[kg/m^3]
$n_{@308nm}$	5.015	1.772	1.73	2.236	
$k_{@308nm}$	3.65	4.091	1.98	0.0324	
T_m	1690	-	1728	2300	[K]

Different Ni thicknesses led to melting of Si at different fluence values. The minimum fluence values at which crystalline Si (c-Si) melting occurs is referred to as ED_{min}. The presence of Ni greatly reduces the reflectance of the liquid c-Si + Ni stack at 308 nm (see Figure 9.4b) compared to liquid c-Si only (R_{308nm}=70%). This results in increased absorption of the laser light and hence melting of Si at the Si/Ni interface at lower fluence thresholds. As a result, simulated ED_{min} drop from 1.6 J/cm^2 for bare Si to 1.2 J/cm^2 for 20 nm of Ni, and down to 1.0 J/cm^2 for Ni thicknesses in the range of 40-100nm. For Ni >>100nm, the laser energy is mostly absorbed into Ni since heat capacity (in J/K) increases with mass and hence higher fluence values are required for Si to melt at the Si/Ni interface. Simulations gave an ED_{min} of 1.4 J/cm^2 for 500 nm of Ni.

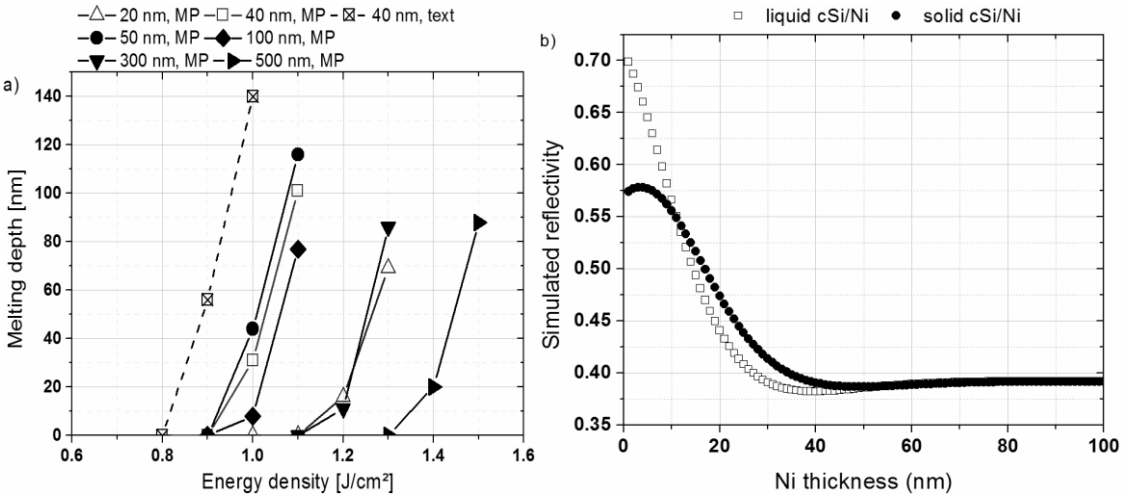


Figure 9.4 a) Simulated Si melting depth on mirror polished Si versus the laser energy density for Ni thicknesses ranging from 20 to 500 nm. Simulation results on random pyramid textured Si for 40nm of Ni are indicated as reference. ED_{min} are taken as the (b) Calculated reflectance at 308nm on mirror polished substrate for liquid c–Si/Ni (□) and solid c-Si/Ni (●) as a function of Ni thickness.

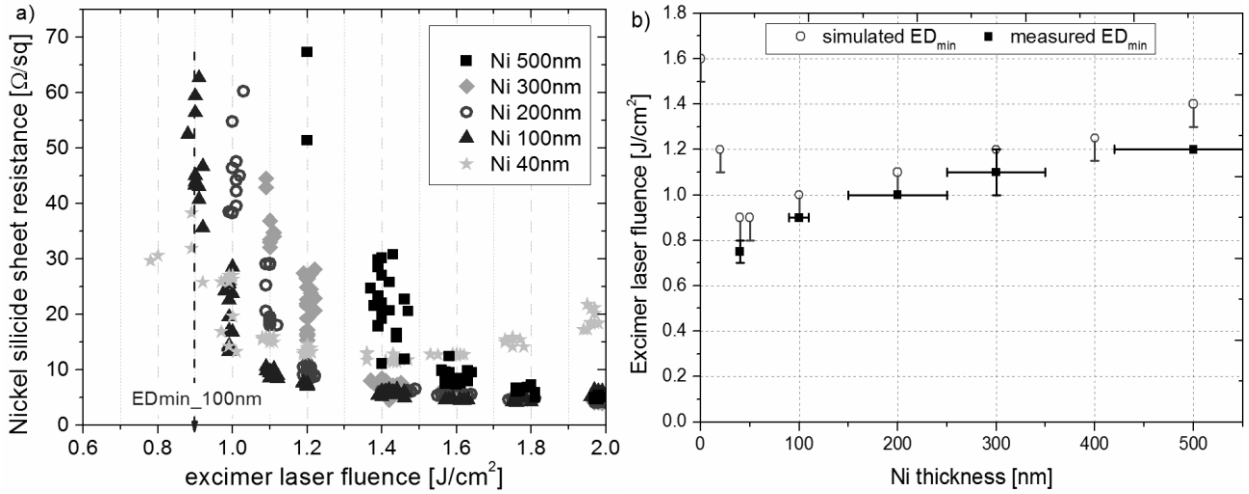


Figure 9.5 a) Sheet resistance (R_{sh}) of nickel silicides formed as a function of excimer laser fluence for various Ni thicknesses on 725-µm thick mirror polished. Unreacted Ni was removed prior to R_{sh} measurement. b) Simulated ED_{min} (○) (i.e. fluence required to melt Si at the interface, taken from Figure 9.4a) and measured ED_{min} (■) (i.e. minimum fluence at which nickel silicides are formed in (a))

To verify the simulated ED_{min}, fluence maps were carried out for Ni PVD thicknesses in the range of 40 nm to 500 nm. Experimental ED_{min} values were defined as the minimum fluence at which nickel silicide formation is detected after unreacted Ni removal (see Figure 9.5a). For each Ni thickness, three mirror polished wafers were simultaneously deposited in the same sputter system. This resulted in some variation in Ni thickness (extracted from R_{sh} on as-deposited wafers) particularly for thick Ni layers as shown in Figure 9.5b. As simulated ED_{min} were defined as the thresholds for Si melting, their close match with experimental ED_{min} supports the fact that nickel silicide formation by ELA occurs in the melt-regime. Most likely, the temperature ramp-up and ramp-down rates experienced by ELA (up to 10^3 ºC/s) do not allow any significant solid-state reactions to occur during ramp-up and ramp-down phases meaning that no significant silicide formation occurs until Si melts at the Si/Ni interface. The incorporation of Ni into the Si melt then drastically reduces the solidification temperature according to the Ni-Si phase diagram (Figure 5.6 in Chapter 5) enabling sufficient time for Ni and Si to mix thoroughly and form either NiSi or $NiSi_2$ phases depending on the amount of Ni incorporated into the melt.

We ran the model as well on mirror polished substrates for c-Si/SiN_x and c-Si/SiN_x/Ni (40 nm) stacks with a SiN_x thickness of 75 nm as typically used in front anti-reflective coating (ARC). Interestingly, Si can melt under 40 nm of Ni at 0.9 J/cm^2 while it remains in solid phase under 75 nm of SiN_x up to 1.1-1.2 J/cm^2 for both c-Si/SiN_x and Si/SiN_x/Ni stacks. This is because the laser light (λ=308 nm) is practically not absorbed in SiN_x (k_{SiNx} ~0) while Si acts as heat sink. These differences in melting thresholds potentially enables full area ELA using large area pulses (10x10 mm^2) and a step-and-repeat approach to form NiSi in the front contact without damaging the emitter passivation and reflectance properties of the neighbouring ARC SiN_x layer. In the next section, we discuss the threshold for emitter passivation damage and compare it to the threshold obtained for NiSi formation in order to define the process window of full area ELA.

9.2.3. Impact of front dielectric(s) thickness

The impact of ELA on emitter passivation properties was evaluated by measuring effective lifetime on symmetrical test structures. Measurements were performed on 5", p-type, 200 Ω.cm, mirror polished FZ-Si wafers in order to compare fluence thresholds for passivation damage (ED_{th}) with ED_{min} values obtained earlier on mirror polished substrates. Wafers were cleaned, diffused (85 Ω/sq emitter) in a $POCl_3$ furnace, cleaned again, and passivated on both sides. Passivation consisted of either: ~15nm thermal oxide grown at low temperature (T~800°C) and a PECVD SiN_x layer (i.e. double ARC or DLARC) or PECVD SiN_x only (i.e. ARC). For both DLARC and ARC the refractive index of SiN_x was ~2.05 and four groups (with 3 wafers per group) were prepared with different SiN_x:H thicknesses (30, 50, 70, and 100 nm). The test structures were fired in a fast firing oven (~800˚C peak wafer temperature) and divided in 9 zones (see Figure 9.6a) subjected to different ELA fluence values. Effective lifetimes τ_{eff} were measured in each zone at $1x10^{15}$ cm^{-3} injection level using quasi-steady state photo conductance calibrated photoluminescence (QSSPC-PL, BTI imaging). ED_{th} values were arbitrarily defined as the fluence values at which τ_{eff} is equal to 90% of τ_{eff} without ELA as shown in Figure 9.6b. Following the same procedure, ED_{th} values were also determined on textured CZ-Si samples.

ED_{th} values obtained on mirror polished FZ-Si vary strongly as a function of SiN_x thickness (Figure 9.6c). For a single ARC, ED_{th} values go from 0.6 J/cm^2 for 30 nm of SiN_x up to 1.2 J/cm^2 for 70 nm and down again to 0.8 J/cm^2 for 90 nm. This is explained by reflectance properties of the SiN_x layer which couples the excimer laser light (λ=308 nm) better into Si when it is 30 nm or 90 nm thick than when it is 70 nm thick. For a DLARC, the maximum reflectance at 308 nm is shifted to thinner SiN_x thus the maximum ED_{th} is shifted to 50 nm of SiN_x.

Knowing the optimum SiN_x thickness required for a single ARC (SiN_x~75-85 nm for n_{SiNx}~2.0) or for a DLARC (SiN_x~50-60 nm for SiO_2~15 nm and n_{SiO2}~1.46), we can determine the process window for full area ELA on planar substrates by comparing the ED_{th} values given in Figure 9.6c with ED_{min} values given earlier in Figure 9.5b. Based on this comparison we find that Ni should be kept between 20 and 200 nm in order to form NiSi without damaging the surrounding passivation. However, ED_{th} values obtained on textured surfaces are only 0.5-0.6 J/cm^2. ED_{th} values are independent of SiN_x thickness for both ARC and DLARC layers which indicates that passivation damage must be controlled by damage created in the pyramid tips. This hypothesis was confirmed by scanning electron microscopy images since pyramid rounding (i.e. Si melting) was observed on these samples for fluence values higher than 0.5-0.6 J/cm^2.

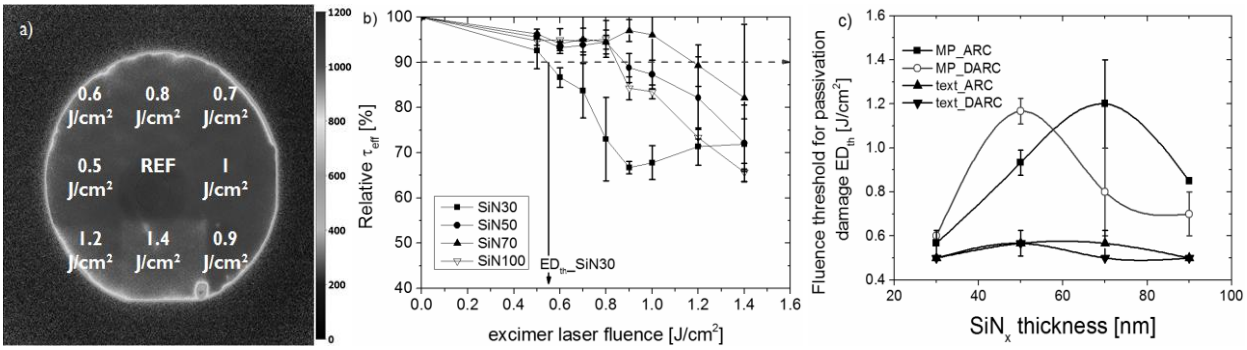


Figure 9.6 a) τ_{eff} map (scale in µs at 1e15 cm^{-3} injection level) of p-type FZ-Si test wafer with 70nm SiN_x for various ELA fluence values. b) Relative τ_{eff} on p-type FZ-Si vs. ELA fluence values for various SiN_x thicknesses. c) ED_{th} vs. SiN_x thickness for single ARC and DARC on mirror polished (MP) or alkaline textured (text) samples.

9.2.4. Proof-of-concept with thin sputtered Ni

Based on previous investigations, a thin (40 nm) sputtered Ni was chosen for proof-of-concept of full area ELA at solar cell level. Large area (12.5x12.5 cm^2) i-PERC type solar cells were fabricated on 1-3 Ω.cm, p-type, CZ-Si wafers. Following wafer cleaning and $POCl_3$ diffusion (80-85 Ω/sq emitter), one-side rear emitter removal was applied in an inline tool. Wafers were cleaned again and passivated on both sides with a thin (~15nm) thermal oxide grown at ~800 ˚C. This was followed by PECVD deposition of SiN_x at the front (i.e. DARC) and $SiOy/SiN_x$ (400/120 nm) at the rear. Local Al-BSF rear contacts were formed by ns-laser ablation of the rear dielectrics, Al PVD deposition (~2 µm), and subsequent firing in an inline furnace.

The front contacts were either co-fired (i.e. reference screen printed (SP) Ag contacts) or Ni/Cu/Ag plated after local Al-BSF formation. In the latter case, the DARC was opened (opening width ~10 µm) by ps-UV laser ablation. Ni was sputtered on top of the entire surface and silicidation was performed by ELA at 0.55 J/cm^2 following a step-and-repeat approach (juxtaposition of 18x18 mm^2 laser shots) to irradiate the entire wafer. Unreacted Ni was selectively removed in a H_2SO_4:H_2O_2 (5:1) mixture and the surface re-activated by a short (30s) 1%HF dip. Contacts were then thickened using consecutive Ni/Cu/Ag plating steps as described in Chapter 5. Finally, the cells were measured and electrical parameters are given in Table 9.2.

We find that that the full area ELA process enables a gain in j_{sc} of 0.8 mA/cm^2 as well as a 0.3 Ω.cm^2 drop in series resistance (r_s) compared to SP-Ag contacts. Plated Ni/Cu/Ag contacts were 30 to 40 µm wide which corresponds to a metal coverage of 3.4 to 4.0% while SP-Ag contacts were around 100 µm wide which corresponds to a metal coverage of 5.8%. These differences in metal coverage translate in a potential 0.72 to 0.98 mA/cm^2 absolute gain in j_{sc} thereby explaining the measured 0.8 mA/cm^2 absolute difference. The 0.3 Ω.cm^2 drop in r_s was found to be solely caused by the change in front size metallization which lead to: (i) a 0.16 Ω.cm^2 reduction in area weighted emitter resistance thanks to more closely spaced Ni/Cu contacts, (ii) reduced line resistance, and (iii) reduced contact resistance as shown in Table 9.2.

Table 9.2: Electrical parameters (illuminated I-V data, pFF from Suns-Voc, specific contact resistance ρc from TLM structures on finished cells) of large area (12.5x12.5 cm^2) i-PERC type cells. Cells feature an industrial 80-85 Ω/sq emitter and front contacts formed by either screen printed (SP) of Ag or excimer laser annealing (ELA) of a thin PVD Ni layer followed by selective Ni etching and Ni/Cu/Ag plating.

Device	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	eta [%]	r_s [$\Omega.cm^2$]	pFF [%]	ρ_c [$m\Omega.cm^2$]
Average SP-Ag (6 cells)	38.3 ±0.1	651.3 ±2.1	77.3 ±1	19.3 ±0.2	1.1 ±0.1	83.2 ±0.3	2.9 ±1.8
best SP-Ag	38.4	653.5	77.8	19.5	1.0	83.4	-
Average Ni/Cu/Ag (ELA) (5 cells)	39.1 ±0.3	649.2 ±1.1	77.7 ±1	19.7 ±0.2	0.8 ±0.2	82.2 ±0.1	0.2 ±0.2
Best Ni/Cu/Ag (ELA)	39.3	649.8	78.3	20.0	0.7	82.1	-

In addition, other characteristics (V_{oc}, pFF) could be maintained to a high level compared to SP-Ag cells. The 2.1 mV drop in V_{oc} and the 1.1%$_{abs.}$ drop in pFF indicate that both the ps-UV laser ablation of the ARC and the full sheet ELA process resulted in very limited emitter passivation and junction damage. Overall, the full sheet ELA process results in a 0.4%$_{abs.}$ increase in efficiency from 19.3% to 19.7%. The best performing cell with this process gave a 20.0% energy conversion efficiency with j_{sc}=39.3 mA/cm^2, V_{oc}=650 mV, and FF=78.3%.

Specific contact resistance (ρ_c) and soldered ribbon pull force measurements (45˚ pull angle, peak force values) were performed since one could argue that ELA at 0.55 J/cm^2 could be insufficient to form NiSi. Results were compared to results obtained with SP-Ag contacts. Adhesion and ρ_c values measured, in a different experiment, on cells featuring a comparable 80-85 Ω/sq emitter before and after conventional RTA are given as reference. In Figure 9.7a, ρ_c values obtained with the ELA process are shown to be significantly lower than with SP-Ag contacts. Values measured are also lower than without any sintering (noRTA) which indicates nickel silicide formation by ELA at 0.55J/cm^2 at cell level. The fact that ρ_c values with ELA (NiSi formation) were not better than values obtained with a conventional RTA at 250˚C (Ni_2Si formation) could indicate that either NiSi is not continuous or that ρ_c values are limited by other processes (surface cleanliness, etc.). Regarding ribbon pull force results, we find that values obtained with the ELA process are about 1.5 N/mm and are comparable with values obtained with RTA.

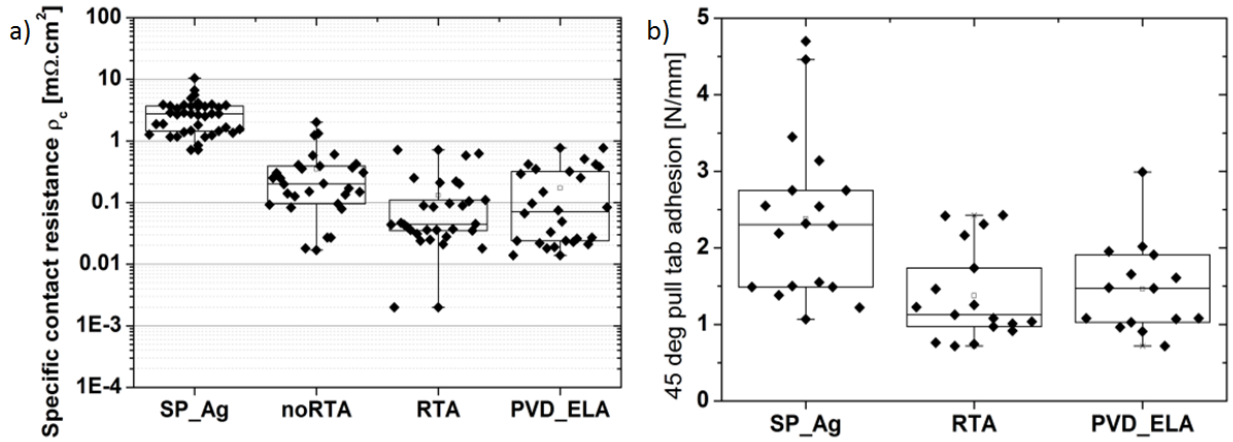


Figure 9.7 a) Specific contact resistance measured on tests structures diced from finished solar cells featuring either screen printed front contacts (SP-Ag), Ni/Cu/Ag plated front contacts before (noRTA) and after rapid thermal annealing (RTA), or sputtered Ni sintered by ELA (PVD_ELA) that were subsequently Ni/Cu/Ag plated. b) Soldered ribbon pull force (45˚ pull angle, peak force values in N/mm) for the various front contact schemes.

9.2.5. Development of a thin bias-assisted LIP Ni layers

Proof-of-concept results with ELA were achieved using a thin (40 nm) PVD Ni layer, to use more industrial Ni deposition methods such as electroless NiP or Light Induced Plating (LIP) we should target 20<Ni<200 nm as shown in the previous section. However, ELA of thin electroless NiP layers were unsuccessful (no silicide formation after unreacted NiP removal). As discussed in Chapter 5.3, electroless NiP in an alkaline bath (pH~10) enables excellent thickness control (deposition rate~80 nm/min) but also results in the formation of an interfacial oxide-rich layer which was shown to delay silicidation by RTA. It is speculated that this interfacial oxide-rich layer blocks silicidation by ELA due to the ultra-short sintering time. Eliminating this interfacial oxide-rich layer (e.g. different chemistry, light assisted electroless NiP) could possibly solve this issue but such trials were not attempted in this thesis. As for bias-assisted LIP Ni, Ni-on-Ni deposition was shown in Chapter 5.4 to be favoured over Ni-on-Si. Uniform ps-UV laser ablation of dielectric(s) on alkaline textured surfaces was also seen as being problematic. Both effects favour Ni nuclei growth and hence it was mentioned that uniform coverage of very thin (<100 nm) Ni layers deposited by bias-assisted LIP could be challenging. Nevertheless, investigations to obtain uniform and thin (<200 nm) Ni layers by bias-assisted LIP were performed during the course of a Master's thesis [ROU13]. Main results are summarized below.

Bias-assisted LIP Ni deposition was first evaluated using a single wafer manual setup shown in Figure 9.8a (8L beaker, sulphamate bath composition given in Chapter 7.2.4). Illumination was obtained by attaching a green LED panel to the wall of the glass beaker. The LED panel consist of 5 rows of 6 LEDs with each LED producing 35.2 lumen when applying 350 mA per row (i.e. 1.75A to the whole panel). A voltage source (resolution 0.01V) was used to apply a protective potential between the rear of the solar cells and the auxiliary anode consisting of two Ti/Pt baskets filled with S-Ni pellets. A metallic clip similar to the one used in the MECO

inline plating tool was used to contact the solar cell (fully immersed in the solution) and keep it in position. Current flowing between the rear of the cell and the auxiliary anode was measured using a Keithley195A digital multi-meter (resolution 0.01A) connected in series. Temperature control was done using a thermostat and a magnetic stirrer was used for agitation.

Measurements were first performed to confirm that the LED panel light intensity increases linearly with applied current. An encapsulated reference cell (52x52mm^2 full Al-BSF) was used as photo-detector by immersing it in the electrolyte at various distances from the LED panel. The reference cell current was found to increase linearly with the current applied to LED panel, as shown in Figure 9.9a, except at 2.5A which is far above the LED panel recommended operating point (1.75A). Since the current generated by the reference cell is proportional to the light intensity A it receives, the absorption coefficient α of the nickel sulphamate bath could be derived from the Beer-Lambert law linking α to I via the incident intensity A_0:

$$A = A_0 e^{-\alpha x} \qquad (9.1)$$

Fitting measured data (see Figure 9.9b) according to (9.1), we obtained $\alpha = 0.12 \pm 0.01\ \text{cm}^{-1}$. Such a small value corresponds fairly well to values given in literature at 550 nm and is due to the fact that nickel electrolyte exhibit the highest transmission for green wavelengths [BAR12].

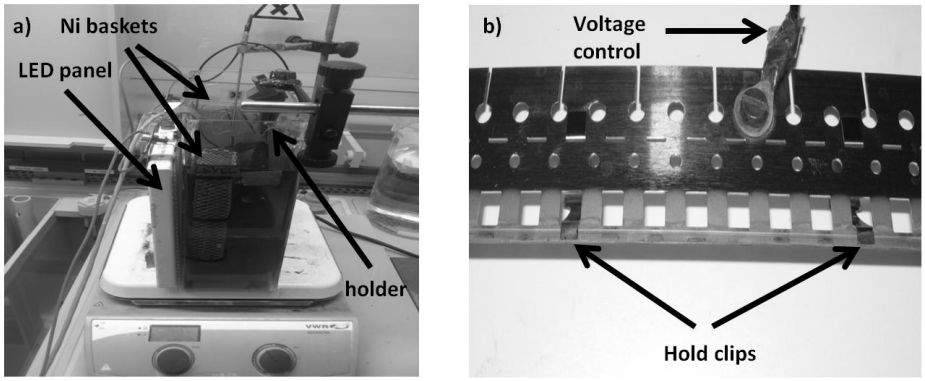


Figure 9.8 a) Manual bias-assisted LIP setup. b) Metallic clip used to contact the rear side of the cell during plating.

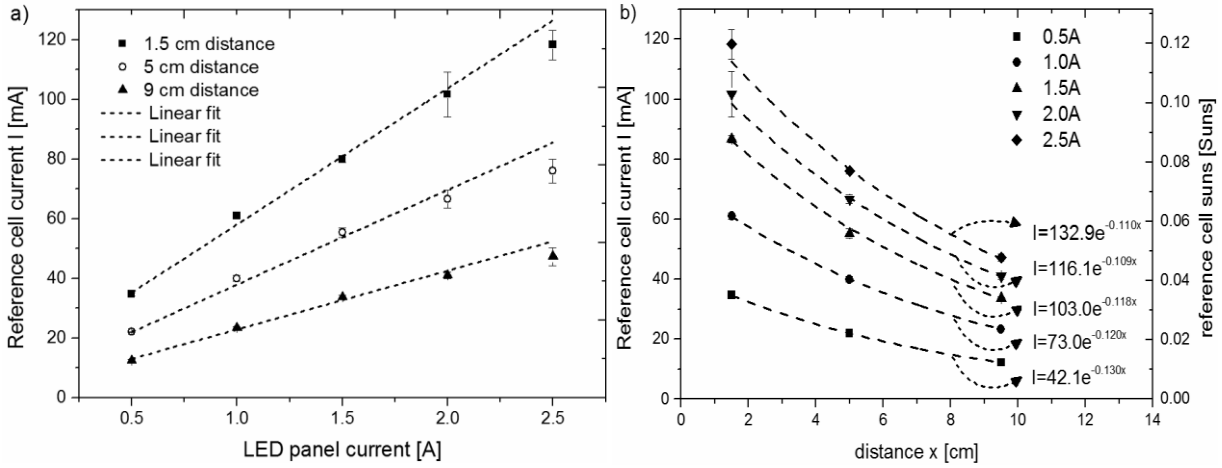


Figure 9.9 a) Measured reference cell current (immersed in the electrolyte) versus LED panel current for various cell-to-LED distances. b) Measured reference cell current versus distance for various LED panel current.

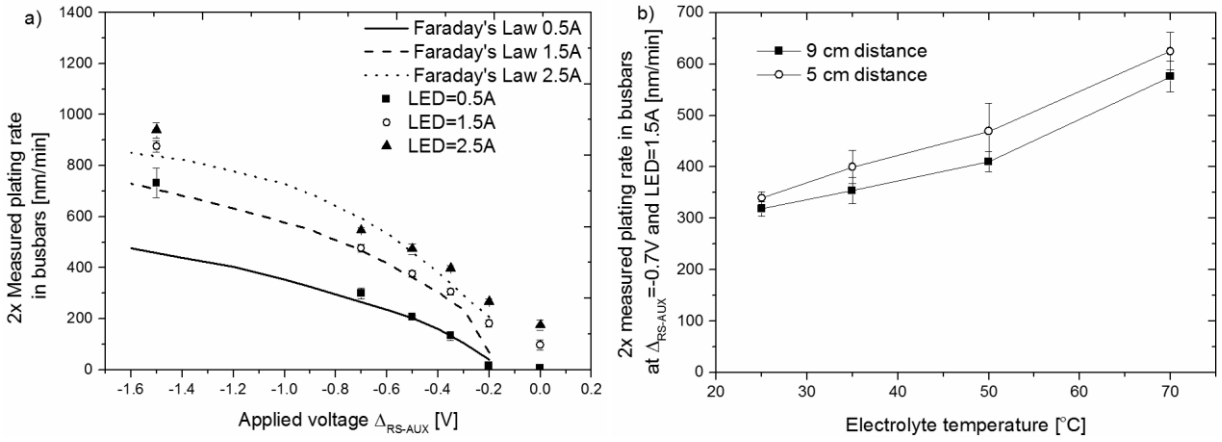


Figure 9.10 a) 2x measured plating rate in busbars (XRF thickness divided by 10min plating time) at T=50˚C versus applied voltage between the rear side and the auxiliary anode ($\Delta_{RS\text{-}AUX}$) for various LED panel current rate. Plating rates derived from Faraday's Law are also indicated. b) 2x measured plating rate in busbars at $\Delta_{RS\text{-}AUX}$=-0.7V, LED=1.5A versus electrolyte temperature for various cell-to-LED distances.

Experiments were then performed to evaluate the impact of applied voltage between the rear side and the auxiliary anode ($\Delta_{RS\text{-}AUX}$) on the plating rate. Electrolyte temperature was kept at 50˚C and cell-to-LED panel distance at 9 cm. Mini-cells (total area: 12.2 cm^2, contact area: A_{cont}=0.49 cm^2) diced from 156x156mm^2 p-type PERC solar cells were used for these tests. Ni plating rate (in nm/min) was determined by measuring the deposited Ni thickness at the front side by X-Ray fluorescence (XRF, see Appendix B) in 4 points along the busbar of each mini-cell and dividing it by the plating duration. Edges were covered with chemical resistant tape to limit edge effects and mini-cells were fully immersed in the electrolyte during plating (note that plating can still occur on the rear Al side of the cells). The measured plating rate was compared to the plating rate r calculated from Faraday's Law (see Chapter 2.2) using I_{LIP} as the average current measured between the rear of the cell and the auxiliary anode during plating:

$$r = \beta \frac{M \cdot I_{LIP}}{\rho_{metal} \cdot A_{cont} \cdot z \cdot F} \tag{9.2}$$

with the molar mass M, the density ρ_{metal}, and the metal ion valence z being 58.71 g/mol, 8.902 g/cm^3, and 2 respectively for Ni. Electrolyte efficiency β was assumed to be 100%.

For protective potentials in the range of -0.2V to -0.7V we found a relative good correlation between the plating rate r derived from Faraday's Law and 2x the measured plating rate in the busbar areas (see Figure 9.10a). Measured Ni thicknesses in finger areas were found consistently 2x higher than in busbars areas (see below) thus Faraday's Law describes fairly well Ni plating in finger areas. It is speculated that the 2x slower plating rates in the busbars are the result of both lower opened fraction (~80-90% instead of 100%) and reduced collection area (~1mm wide busbars as compared to ~10µm wide fingers). Measured plating rates deviated significantly from Faraday's Law for very high cathodic potentials ($\Delta_{RS\text{-}AUX}$=-1.5V) which also correspond to the region where significant plating was observed at the rear side. As mentioned in Chapter 5.4.1, the assumption that I_{LIP} describes only plating at the front side is no longer valid in this region since I_{LIP} becomes the cumulative current between front side and anode, and rear

side and anode. Therefore, we do not expect the plating rate derived from I_{LIP} to be accurate in this region. Very low protective potentials ($\Delta_{RS\text{-}AUX}$>-0.2V) are also not ideal since significant dissolution of the rear Al can occur. In addition, the presence of shunts or edge effects may have a more pronounced effect on the front side potential and hence on Ni thickness distribution. Overall, slower plating rates were obtained for lower LED panel current (i.e. lower light intensity) which supports the fact that plating rates are limited by the current generated by the solar cell in the electrolyte.

Reducing the electrolyte temperature from 50˚C to 25˚C proved to be beneficial as lower plating rates could be obtained with better thickness uniformity (see Figure 9.10b). The lower plating rates at 25˚C are the result of both increased resistivity [ROU13] and increased viscosity leading to slower replenishment of metal ions [DUR84]. Further lowering the temperature below 25˚C was seen as not viable since this led to incomplete dissolution of boric acid.

Following these investigations at beaker level, several parameters were fixed (T=25 ˚C, $\Delta_{RS\text{-}AUX}$=-0.4V, LED=0.5A) and tests were done in the MECO inline plating machine (identical sulphamate bath) to benefit from non-static deposition and more uniform cell-to-LED distance.

Tests were first done with default settings (bath length=0.9 m, belt speed=0.3m/min) leading to a deposition time of 180s. This resulted in Ni>300 nm as shown in Figure 9.11a. Also shown in this figure are the good agreement between XRF and SEM data for Ni thickness determination and the thickness ratio ~2 between fingers and busbars. Such thickness differences can also be visualized in SEM images shown in Figure 9.12. Keeping other deposition parameters constant, the deposition time was reduced by pulsing the LED panels (ON/OFF time: 0.1s/0.3s) to achieve an effective deposition time of 45s which led to the target 20<Ni<200 nm in both finger and busbars areas. These results were reproduced on four full area 156x156 mm^2 substrates that were plated consecutively (see Figure 9.11b). Reducing deposition time further (longer OFF time or faster belt speed) led to insufficient Ni coverage in the busbars (see Figure 9.12(c) and (d)). ELA 156x156mm^2 cell results with pulsing “45s” are presented in next sections.

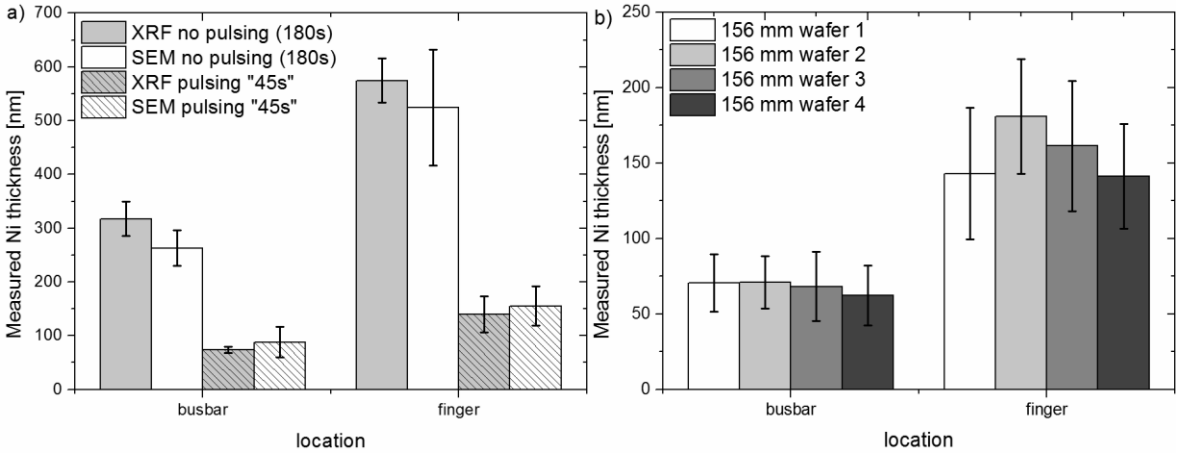


Figure 9.11 a) Measured Ni thickness (determined by XRF or SEM) after plating at $\Delta_{RS\text{-}AUX}$=-0.4V, LED=0.5A, T=25˚C in the MECO tool for different durations. b) Measured Ni thickness (XRF) after plating 156x156mm^2 cells in the MECO tool at $\Delta_{RS\text{-}AUX}$=-0.4V, LED=0.5A, T=25˚C, and using pulsing “45s” (i.e. ON/OFF time: 0.1s/0.3s).

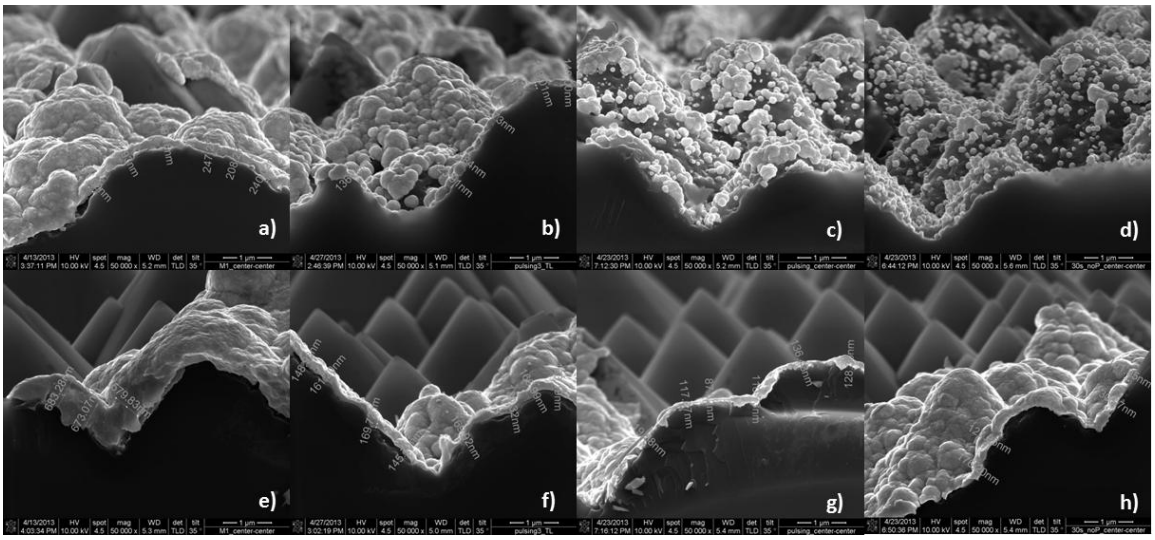


Figure 9.12 Scanning electron microscopy (SEM images) at $\Delta_{RS\text{-}AUX}$=-0.4V and LED= 0.5A after bias-assisted LIP Ni plating in the MECO tool at 25˚C for various plating duration. SEM images in busbar areas: a) no pulsing, 120s, b) pulsing "45s" (i.e. ON/OFF time: 0.1s/0.3s), c) pulsing "30s" (i.e. ON/OFF time: 0.1s/0.5s), d) no pulsing, 30s. SEM images (e) to (h) are taken in finger areas and correspond to conditions applied in (a) to (d) respectively.

9.2.6. Impact of front junction depth

The impact of junction depth was evaluated as reduced j_{02} recombination in shallow junction devices was presented at the beginning of this chapter as a possible advantage of ELA. Following proof-of-concept of ELA on solar cells featuring an industrial 80-85 Ω/sq emitter (see section 9.2.4), experiments were performed on 15.6x15.6cm^2 PERC type solar cells featuring a shallow (~0.3 µm) ~130 Ω/sq emitter (SIMS profiles are given in Chapter 6.2). The process sequence to fabricate these cells was identical to the one given in section 9.2.4 except for the different substrate size and the different $POCl_3$ diffusion recipe. All cells featured Ni/Cu/Ag plated front contacts. A comparison was made between sintering at the end (BTU, 250˚C, 4min) or sintering directly after thin (40 nm) PVD Ni deposition (ELA: 0.55 J/cm^2 or RTA=300˚C, 30s). For the latter, unreacted Ni was selectively etched in H_2SO_4:H_2O_2 (5:1), the surface re-activated by a short (30s) 1%HF dip, and the contacts were thickened (Ni/Cu/Ag plating).

Comparable cell results were obtained using either ELA or RTA for the silicidation of the thin (40 nm) PVD Ni layer while cells sintered at the end performed worst (see Table 9.3). These cells performed worse mostly because of lower V_{oc} and lower J_{sc} values which we could not explain. All groups were limited by relatively high series resistances values (r_s~1 Ω.cm^2) and poor pseudo fill-factors values (pFF~81.8%). Excellent specific contact resistance (ρ_c<0.1 mΩ.cm^2) were measured (see Chapter 6.2) thus we attribute high r_s values to insufficient plating (finger resistance) and non-optimum grid design (emitter resistance). The fact that pFF~81.8% were measured already prior to sintering highlights the fact that j_{02} recombination in these cells is not limited by the sintering technique but rather by damage created during ps-UV laser ablation (this was further evidenced in Chapter 6.2). From these results it is also not possible to determine if ELA yields any advantage over RTA for solar cells featuring a shallow (~0.3 µm) junction.

Table 9.3: Electrical parameters of large area (15.6x15.6 cm^2) i-PERC type cells. The cells feature a shallow (~0.3 µm) ~150 Ω/sq emitter and Ni/Cu/Ag plated front contacts. Sintering is either performed at the end (BTU tool 250˚C, 4min) or directly after thin (40 nm) PVD Ni deposition (ELA:0.55 J/cm^2 or RTA=300˚C, 30s)

Device (4 cells/group)	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	eta [%]	r_s [Ω.cm^2]	pFF [%]
Ni/Cu/Ag no BTU	39.5±0.1	645.0±1.7	75.8±1.0	19.3±0.3	1.1±0.2	81.8±0.1
best	39.6	646	75.8	19.4	1.10	81.8
Ni/Cu/Ag BTU	39.4±0.1	644.5±2.1	76.3±0.8	19.4±0.2	1.0±0.2	81.9±0.1
best	39.4	644	77.1	19.6	0.86	81.9
PVD Ni_RTA_Ni/Cu/Ag	39.6±0.1	648.0±1.4	76.6±1.1	19.7±0.3	0.9±0.2	81.8±0.1
best	39.6	650	77.7	20.0	0.72	81.8
PVD Ni_ELA_Ni/Cu/Ag	39.6±0.0	646.7±0.6	76.8±0.7	19.6±0.2	0.9±0.1	81.7±0.3
best	39.6	647	77.6	19.9	0.76	82

ELA and RTA were further compared on cells featuring a 0.5 µm deep 120 Ω/sq emitter (SIMS profile given in Chapter 6.2). Cell results with conventional RTA at the end (BTU tool, 250˚C, 240s) have already presented at the end of Chapter 5. Results given below with ELA were obtained on sister cells that were co-processed up to ps-UV laser ablation of the front dielectrics. After ps-UV laser ablation, a thin Ni layer was deposited by bias-assisted LIP Ni in the MECO tool (plating "45s", see previous section) and ELA was performed at 0.55J/cm^2.

Solar cells featuring nickel silicides contacts sintered by ELA resulted in lower j_{sc}, V_{oc}, and FF than cells sintered at the end in the BTU tool. The lower j_{sc} were attributed to parasitic plating that was lightly visible on the cells. Scanning electron microscopy (SEM) taken directly after ELA of thin LIP Ni layer indicated that front dielectrics were removed in few of the pyramid tips (see Figure 9.12). It is speculated that parasitic plating during subsequent Ni/Cu/Ag occurred at these locations. Damage at the pyramid tips is also likely to explain the ~2 mV drop in V_{oc}. As discussed in section 9.2.3, the chosen ELA at 0.55 J/cm^2 is at the edge of passivation damage. Reducing the fluence to 0.50 J/cm^2 or below could solve this issue but might result in insufficient silicidation. For the present 0.55J/cm^2, we could confirm nickel silicide ($NiSi_x$) formation after unreacted Ni removal from both SEM images (white contrast in SEM images due to $NiSi_x$ being more conductive than Si) and XRF measurements (detection of Ni from $NiSi_x$). It is interesting to note that the recipe developed for thin Ni deposition seems to be reproducible and that Ni silicidation by ELA occurs mainly at the pyramids tips as described previously.

Overall, these results demonstrate that ELA of thin LIP Ni layers enables the fabrication of large area p-type PERC solar cells with average efficiencies ~ 20.2%. Though these results are encouraging for a first trial, they are $0.3\%_{abs.}$ lower than with RTA at the end. ELA also introduces extra complexity (ELA tool, need 20<Ni<200 nm, no sintering at the end, risks of passivation damage) which, so far, cannot be justified since it was not possible to determine if ELA yields an advantage over RTA for ~0.3 µm junctions that would be cheaper to manufacture.

Table 9.4: Electrical parameters (illuminated I-V data, r_s from 2 light-level, pFF from Suns-Voc) of large area (15.6x15.6 cm^2) i-PERC type cells. The cells feature a ~0.5 µm deep 120 Ω/sq emitter and Ni/Cu/Ag plated front contacts. Sintering is either performed at the end (BTU tool 250˚C, 4 min) or directly after LIP Ni (ELA:0.55J/cm^2)

Device	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	eta [%]
Ni/Cu/Ag BTU (109 cells)	38.8±0.1	661.3±1.2	80.0±0.2	20.5±0.1
best	39.1	661.7	80.0	20.7*
LIP Ni_ELA_Ni/Cu/Ag (5 cells)	38.6±0.1	659.0±0.7	79.6±0.1	20.2±0.0
best	38.6	659.0	79.7	20.3

*Externally confirmed at FhG ISE CalLab

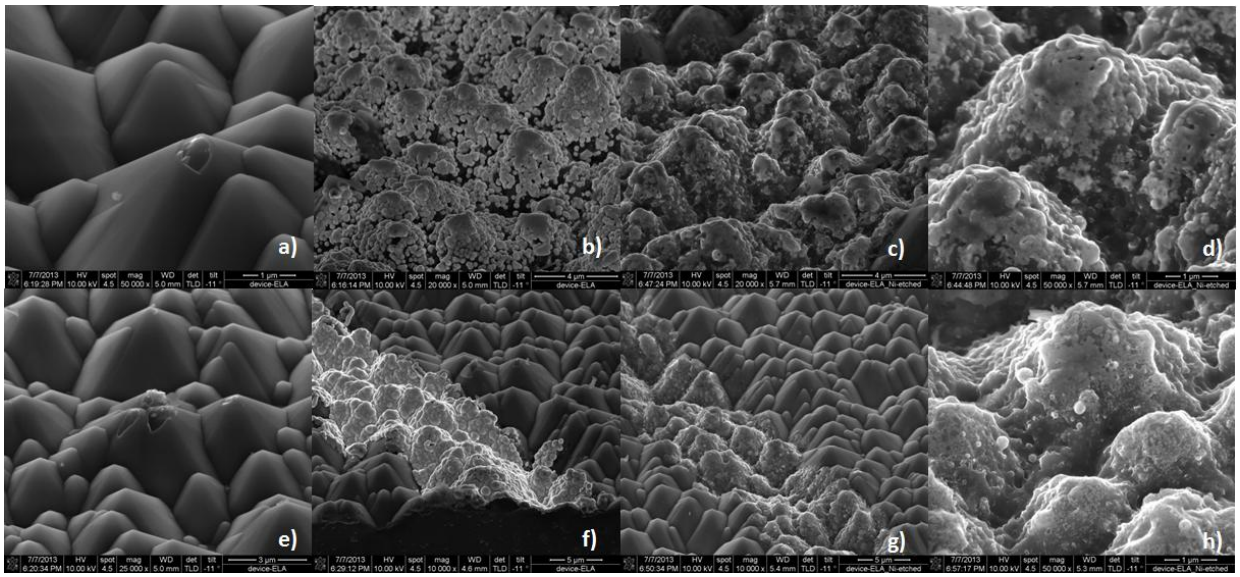


Figure 9.12 Scanning electron microscopy (SEM images) in (a) and (e) show evidence of dielectric removal at pyramid tips after ELA at 0.55J/cm^2 in un-metallized areas. SEM images of LIP Ni (plating "45s") in busbar before (b) and after (c) + (d) unreacted Ni etch, and in a finger before (f) and after (g) + (h) unreacted Ni removal.

9.3. Excimer laser annealing in hybrid rear junction n-type PERT cells

9.3.1. Motivation

Silicon heterojunction (SHJ) solar cells based on an n-type crystalline c-Si(n) wafer and intrinsic and doped hydrogenated a-Si:H layers on both sides are attracting a lot of interest owing to their ability to enable V_{oc} values well beyond 700 mV with a simple one dimensional (1D) design [HER12, MUN12, BAL13]. However, SHJ solar cells suffer from parasitic absorption in the a-Si:H layers and transparent conductive oxide (TCO), particularly at the illuminated side, which leads to a trade-off between V_{oc}, j_{sc}, and FF [HOL12]. To overcome this issue, intrinsic and boron doped a-Si:H layers forming the SHJ emitter can be deposited at the rear side and a front surface field (FSF) formed at the illuminated side either by field-effect passivation [WUN06] or by diffusion [BIV10, BIV12]. Using the latter approach and a blanket rear Ag

electrode, efficiencies up to 22.8% with j_{sc} =39.9mA/cm^2, V_{oc}=705mV, and FF=81.2% were reported on 4cm^2 n-FZ-Si [BIV12]. Front contacts were defined by lift-off (i.e. photolithography patterning) of an evaporated Ti/Pd/Ag stack followed by Ag plating. Also no sintering was applied to the Ti/Pd/Ag contacts in these cells to improve contact resistance as degradation of the SHJ emitter has been reported for annealing temperatures >200˚C [deW10].

As mentioned earlier in this chapter, excimer laser light is absorbed in the near-surface region. In IC, this opened the possibility for dopant activation by ELA without damaging layers present a few μm below the surface [VEN12]. In PV, this opens the possibility for a n-PERT cell design where the boron diffused rear emitter would be replaced by a SHJ emitter and silicidation of the self-aligned Ni plated front contacts performed by ELA before Cu plating. Such a cell architecture is referred hereafter as hybrid n-PERT. Proof-of-concept results are discussed next.

9.3.2. Proof-of-concept

Both the homo-junction n-PERT (see Chapter 8) and hybrid n-PERT feature an identical front side as shown in Figure 9.13. The hybrid n-PERT potentially combines reduced parasitic absorption and reduced shading losses at the front side with the advantages of SHJ solar cells (simple 1D design, excellent surface passivation) at the rear side. The optimum rear stack in hybrid n-PERT depends on the surface roughness. For a mirror polished rear side, it is possible to deposit Ag directly on the SHJ emitter while achieving high j_{sc} and FF above 80% [BIV12]. However, doing so on a chemically polished (i.e. rough) surface would lead to significant j_{sc} losses due to absorption at the interface with Ag [KIM11]. One approach to minimize j_{sc} losses in such surfaces is to require the rear TCO (in between the SHJ emitter and rear metal electrode) to serve both as contact layer and optical buffer by making it relatively thick and infra-red (IR) transparent [HOL12]. A more complex approach is to use a thin TCO only as contact layer and insert an additional layer that is specifically chosen as optical buffer [HOL13a]. Combining the latter approach with the ability of SHJ emitter to passivate textured surfaces it becomes possible to obtain high V_{oc} together with extremely good IR internal quantum efficiencies [HOL13b].

Following literature study, proof-of-concept of the hybrid n-PERT concept was done on cells featuring a relatively thick indium tin oxide (ITO) and a Ag rear electrode. A comparison was made between chemically rear polished surface, as currently used in n-PERT, and textured rear as the latter potentially enables improved light trapping and a simpler process sequence. A control group was added so that we could evaluate the impact of conventional nickel silicidation by RTA (BTU tool, 250˚C, 240s). Additional control groups were included with the entire rear stack (a-Si:H(i)/a-Si:H(p)/ITO/Ag) deposited at EPFL instead of at imec. At both locations, PECVD deposition times a-Si:H layers were adapted depending the rear surface morphology. However, only the I-V results obtained with cells part-processed at EPFL are presented below since I-V results obtained with imec layers were about 1%$_{abs.}$ lower in efficiency due to lower j_{sc}.

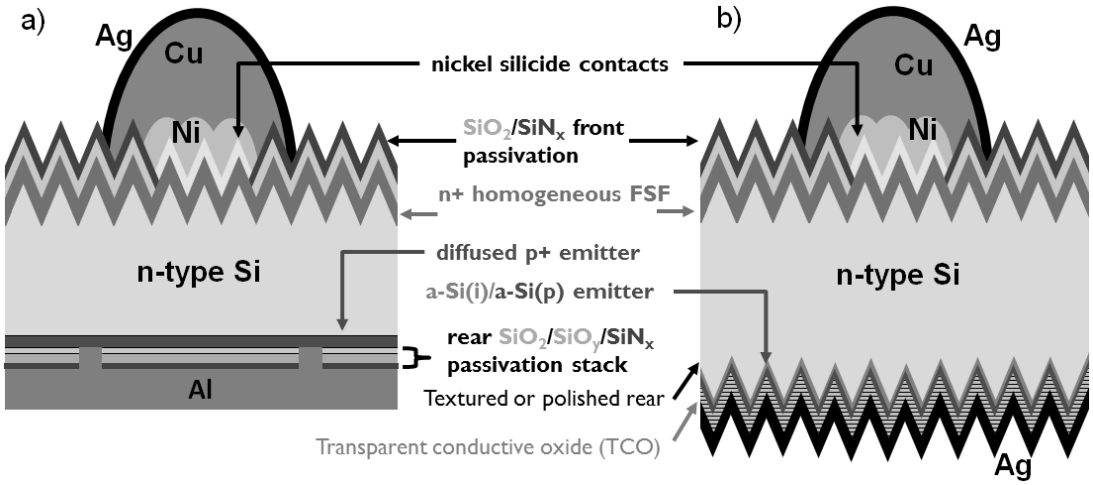


Figure 9.13 Schematic of: a) homo-junction n-PERT with a boron diffused rear emitter (see Chapter 8) and b) hybrid n-PERT with an heterojunction rear emitter (rear stack: a-Si:H(i)/a-Si:H(p)/ITO/Ag).

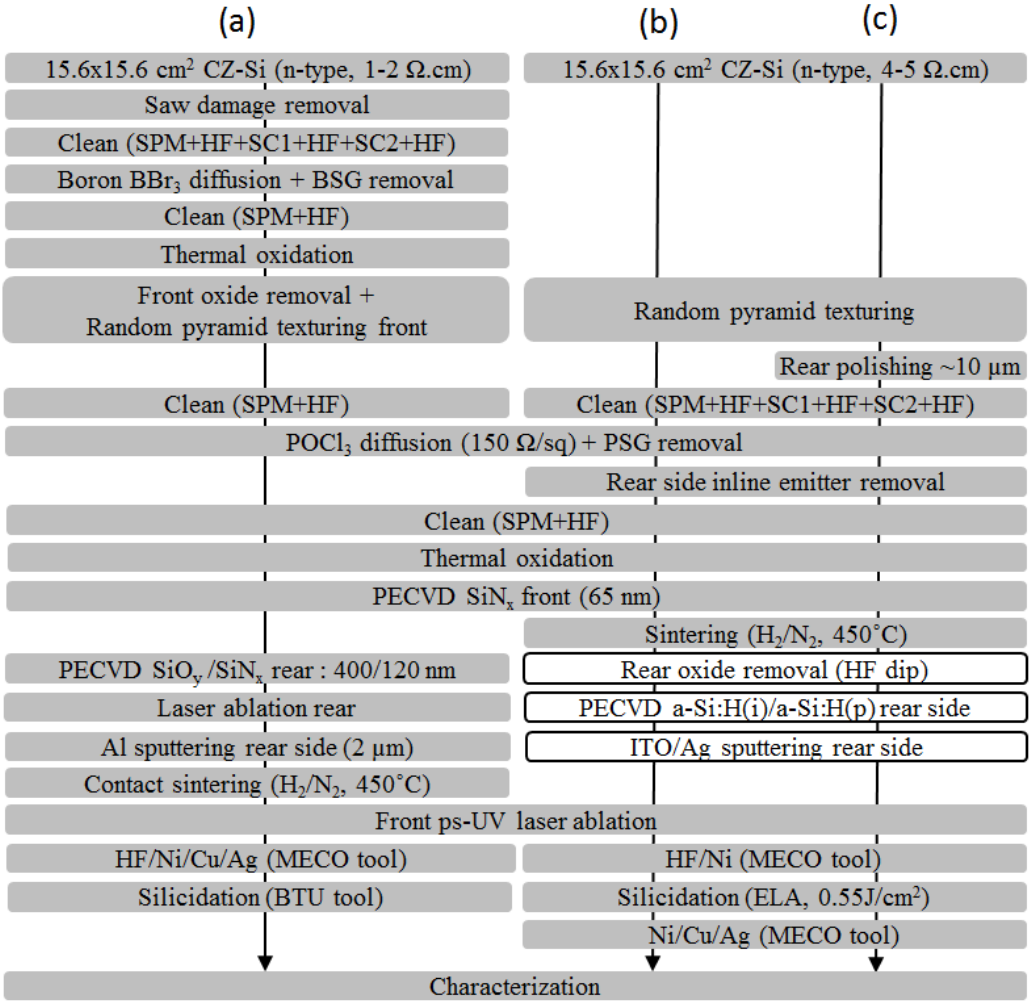


Figure 9.14 Process sequence for: a) homo-junction n-PERT with a boron diffused rear emitter (see Chapter 8) and b) hybrid n-PERT featuring an heterojunction rear emitter, steps with a white background were performed at EPFL.

The process sequence used to fabricate large area (15.6x15.6 cm^2) hybrid n-PERT for proof-of-concept is shown in Figure 9.14 where it is compared to one for homo-junction n-PERT cells presented in Chapter 8. Other than the rear emitter sequence and the front metallization sequence, the main differences are: (i) the higher resistivity substrates (4-5 Ω.cm) and (ii) the poorer reflectance results in this particular experiment (~14±1% at 700nm as compared to the 10.5±1% normally achieved). As discussed in Chapter 6.1, dark saturation current density (j_0) contributions were obtained from QSSPC-PL measurements on co-processed test wafers.

We can clearly demonstrate the proof-of-concept of hybrid n-PERT solar cells from the average cell results given in Table 9.5. Cells where silicidation of the self-aligned Ni plated front contacts was performed by ELA gave comparable V_{oc} as cells that did not receive any sintering. Conventional RTA at 250˚C resulted in a strong degradation of all cell parameters which provides evidence that silicidation by ELA is a one-side heating process. Hybrid n-PERT cells featuring a polished rear side are found to be mainly limited by high series resistance (r_s=1.9 Ω.cm^2) leading to FF values around 74%. This compares to r_s=0.5 Ω.cm^2 and FF around 80% for conventional n-PERT cells. Though bulk resistivity was higher (4-5 Ω.cm) in hybrid n-PERT than in n-PERT (1-2 Ω.cm), its effect is considered to be negligible since majority carrier transport in the bulk is 1D. Both n-PERT and hybrid n-PERT feature FSF sheet resistances ~100 Ω/sq, an identical front grid spacing, and were Ni/Cu/Ag plated to the same thickness. Therefore, hybrid n-PERT cells must be limited by higher series resistance at the rear side.

Hybrid n-PERT cells with a chemically polished rear side most likely suffered from too thick a-Si:H layers since hybrid n-PERT cells with textured rear side gave r_s values 0.5 Ω.cm^2 lower in average leading to FF~77%. However, the latter cells also suffered from lower pFF values which indicates that there might be some trade-off between high FF and low r_s. Nevertheless, these cells gave comparable V_{oc} and j_{sc} values 0.5 mA/cm^2 higher (0.8mA/cm^2 for cells with no ELA) leading to efficiencies around 20.2%. The higher j_{sc} are the result of better light trapping for a textured rear side. As described previously, the 0.2 mA/cm^2 lower j_{sc} for cells with ELA is attributed to parasitic plating due to damage at pyramid tips caused by ELA. While the rear surface is well passivated ($j_{0e,rear}$~10 fA/cm^2 for planar and textured rear side), recombination at the FSF was higher than expected ($j_{0,FSF,pass}$~70 fA/cm^2 as compared to $j_{0,FSF,pass}$~50 fA/cm^2 obtained on n-PERT in Chapter 8). Hybrid n-PERT are mostly limited by recombination under the front contacts as with n-PERT. Assuming $j_{0,FSF,metal}$~1500 fA/cm^2 and considering a metallized area fraction of 2.9% we find a total $j_{0,FSF}$~112 fA/cm^2 which accounts for 80% of all V_{oc} losses. Finally, going to $j_{0,FSF,pass}$=50 fA/cm^2 and using floating busbars we could expect V_{oc} ~690 mV.

Table 9.3: Average (3 cells/group) parameters of large area (15.6x15.6 cm^2) hybrid n-PERT cells with self-aligned Ni/Cu/Ag plated front contacts and a-Si:H(i)/a-Si:H(p)/ITO/Ag at the rear. Sintering is either performed at the end (BTU tool 250˚C, 4min) or directly after LIP Ni deposition (ELA:0.55 J/cm^2). Average results presented in Chapter 8 with standard n-PERT cells (polished rear surface, BBr3 diffused rear emitter) are given as reference.

rear surface	annealing	j_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	eta [%]	r_s [$\Omega.cm^2$]	pFF [%]
polished	ELA	38.1±0.1	680.3±1.5	73.6±0.6	19.1±0.2	1.9±0.2	82.9±0.2
textured	ELA	38.6±0.0	678.5±2.1	77.1±0.1	20.2±0.0	1.0±0.1	81.9±0.2
textured	no anneal	38.8±0.2	676.0±1.0	77.0±0.3	20.2±0.1	0.9±0.0	81.3±0.4
textured	BTU	38.0±0.2	669.7±2.1	72.9±1.2	18.6±0.4	1.5±0.1	80.0±1.1
n-PERT	BTU	37.9±0.4	674.0±2.0	80.1±0.7	20.4±0.1	0.5±0.1	82.7±0.3

9.3.3. Understanding losses upon conventional annealing

Hybrid n-PERT show the same sensitivity to front surface recombination as n-PERT cells (both cells share the same front side) with internal quantum efficiency (IQE) values being much lower for wavelengths up to 1000nm (see Figure 9.15a). Interestingly, the hybrid n-PERT cell with a textured rear side that received conventional RTA at 250˚C has a much lower IR-IQE and a much lower total escape reflectance at 1200nm than a cell with an identical rear side that received ELA. The lower IR-IQE corresponds well with the lower V_{oc} after RTA due to degradation of the rear SHJ emitter. The fact that less light escapes at front side is consistent with the fact that more light is parasitically absorbed in the rear a-Si:H(i)/a-Si:H(p)/ITO/Ag stack. Transmittance and reflectance measurements were performed for increasing annealing temperatures (T_{anneal}) on 2 side polished c-Si(n) wafer. The wafers had a-Si:H(i) at the front side and a-Si:H(i)/a-Si:H(p)/ITO or a-Si:H(i)/a-Si:H(p) at the rear side. Changes in resistivity of the ITO layer were also monitored by four point probe measurements with increasing T_{anneal}. While we did not observe any significant differences in absorption (i.e. 1-transmittance-reflectance) for a-Si:H layers only, samples with ITO led to a significant increase in absorption at long wavelengths for T_{anneal}>200˚C (see Figure 9.15b). Since the resistivity dropped from ~$1x10^{-2}$ Ω.cm prior to anneal to ~$6x10^{-4}$ Ω.cm after annealing at 250˚C, we attribute the increase in absorption at long wavelengths to increased free-carrier absorption in the ITO layer [HOL12a].

Based on these findings, nickel silicidation of the front contacts by ELA appears to offer a significant advantage over conventional RTA since it enables the use of layers (a-Si:H, ITO) that see their properties degrade significantly beyond 250˚C. However, it should be mentioned that alternative hybrid cell structure have recently been demonstrated with rear passivation layers that can withstand temperatures up to 400˚C [FEL13, LI13. STE13]. Similarly, it might be possible to tune the properties of a-Si:H and TCO layers to make them compatible with RTA.

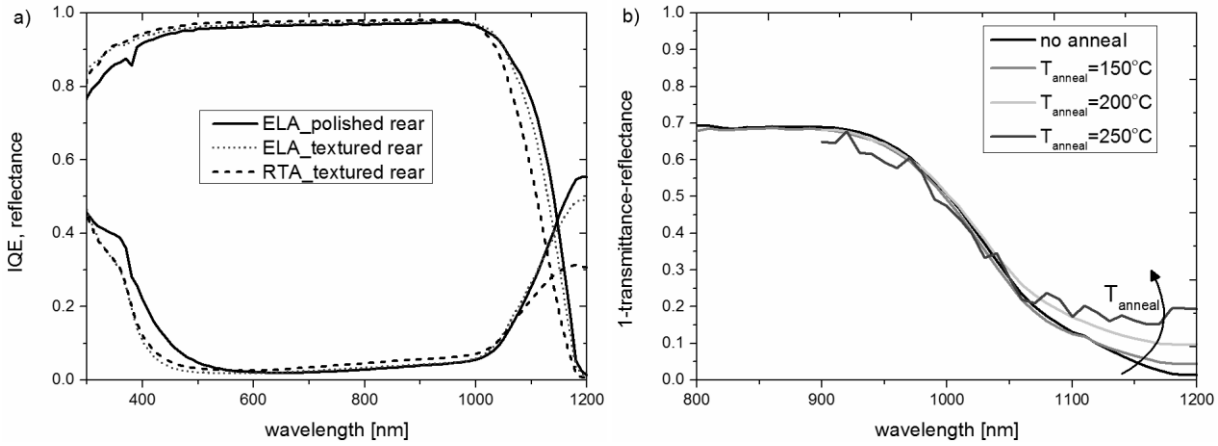


Figure 9.14 a) Internal quantum efficiency (IQE) and reflectance curves (2x2cm^2 spot size) of hybrid n-PERT cells with sintering of the front plated contacts performed after Ni/Cu/Ag plating (RTA 250˚C, 4min) or after LIP Ni deposition (ELA). b) 1-transmittance-reflectance (i.e. absorption) of 2 side polished n-CZ wafers with a-Si:H(i) at the front and a-Si:H(i)/a-Si:H(p)/ITO at the rear for increasing annealing temperatures (T_{anneal}).

9.4. Chapter summary

In this chapter we presented an alternative nickel silicidation method to conventional RTA that we referred to as excimer laser annealing (ELA). ELA is based on a single ultra-short ~180 ns excimer UV-laser pulse leading to nickel silicide formation at the interface between nickel and silicon in either melt or non-melt regime. It was mentioned that nickel silicide formation by ELA could potentially enable: (i) improved control of nickel silicide phase formation, (ii0 reduced j_{02} recombination on shallow emitter devices, and (iii) the use of passivation schemes at the rear side that cannot withstand RTA temperatures.

In the first part of this chapter we evaluated nickel silicide formation by ELA in p-type PERC solar cells. Both reflectance and Ni thickness were shown to have a significant impact on the ELA fluence thresholds for nickel silicide formation. In particular, we could demonstrate that nickel silicidation by ELA on random pyramid textured surfaces led to silicon melting (pyramid rounding) at low fluence values and direct monosilicide (NiSi) formation. Based on finite element simulations we found a close match between the fluence thresholds for melting Si underneath a thin Ni layer and experimental fluence thresholds for nickel silicide formation. This data supports the fact that ELA enables excellent control (thickness, phase) of nickel silicide formation and provides evidence that it is closely linked to liquid-state diffusion unlike conventional RTA which follows solid-state diffusion. Interestingly, we found that it was possible to form nickel silicide by ELA without damaging significantly the properties of the surrounding dielectric layers for Ni layers in the range of 20 to 200 nm. We then evaluated the deposition of thin Ni layers (20<Ni<200 nm) by bias-assisted LIP Ni as an alternative method to sputtering and the impact of several deposition parameters (protective potential, light intensity, electrolyte temperature, etc.) was evidenced. Using thin bias-assisted LIP Ni layers we obtained efficiencies average efficiencies ~20.2% on large area p-type PERC cells. However, it was

mentioned that ELA introduces extra complexity as compared to conventional RTA. We also could not demonstrate any benefit with ELA for ~0.3 µm junctions since results on such junctions were limited by damage created during ps-UV laser ablation of the front side pattern.

In the second part of this chapter, we evaluated an alternative n-PERT cell design where the boron diffused rear emitter was replaced by a heterojunction emitter and silicidation of the self-aligned Ni plated front contacts was performed by ELA. Efficiencies up to 20.2% were obtained in a first trial on large area substrates with V_{oc} up to 680mV and excellent $J_{0,rear}$~10 fA/cm^2 on textured surfaces. We could show that ELA, unlike conventional RTA, did not degrade the properties of the rear stack (a-Si:H(i)/a-Si:H(p)/ITO/Ag) and we could link increased absorption at long wavelengths after RTA to increased free-carrier-absorption in the ITO layer. Finally, we also mentioned that novel hybrid concept which can withstand temperatures up to 400˚C have recently been demonstrated with efficiencies above 23% [FEL13]. Such results clearly show that hybrid cells, that combine simple 1D design and excellent surface passivation at the rear side with reduced absorption and shading losses at the front side, are the way to fully benefit from the advantages of self-aligned Ni/Cu plated front contacts.

CHAPTER 10

Cost of ownership calculations

The aim of this chapter is twofold: (1) to estimate from cost of ownership (CoO) and from return on investment (ROI) calculations if the simplified plating sequence developed in this thesis can be beneficial compared to state-of-the-art silver screen printed front contacts (SP-Ag), and (2) to estimate if this remains the case even when considering drastic reductions in Ag consumption that advanced interconnection techniques could potentially enable.

10.1. Motivation

The simplified plating sequence to define front contacts consists of: (i) laser ablation of the front dielectrics, (ii) a HF/Ni/Cu/Ag sequence that can be performed in an inline plating tool, and (iii) a sintering step under N_2 than can be performed in an inline belt furnace. This sequence was integrated in: p-type PERC (chapters 5 and 6), n-type PERT (chapter 8), and hybrid n-PERT (chapter 9). All three cell concepts introduce several extra steps (e.g. thermal oxidation) as compared to industrial p-type full Al-BSF solar cells with SP-Ag front contacts that would need to be considered in CoO calculations. On the other hand, efficiencies close to 21% could be demonstrated on industrial size substrates with the first two concepts while an efficiency potential close to 22% was estimated for the last two concepts. As these cells were designed to benefit from the excellent contact properties of Ni/Cu/Ag plated contacts, direct comparison with identical cells featuring SP-Ag front contacts was not possible. Therefore, rather than calculating CoO in €/Wp for the entire process flow, the approach taken was to calculate the front metallization CoO per cell of this simplified plating sequence and compare it to the one for printing Ag contacts. Similarly, only additional investments needed for replacing a Ag printing tool by a trio of systems (laser + plating + sintering) and the cost reductions that could be expected from CoO results were considered in return on investments (ROI) calculations.

10.2. Input data

A standardized CoO-model based on SEMI Standards E35, E10 and E79 [ITR13] is used to calculate the cost of: (i) depreciation, (ii) floor space, (iii) materials and consumables, (iv) utilities, (v) waste disposal, (vi) labor, and (vii) yield loss. Summing up the various components gives an front metallization cost for the different steps and for which are given in €/cell.

Annual depreciation cost is obtained from the listed tool price (see Table 10.1) which is fully depreciated over five years. Characteristics for the laser, belt furnace sintering, and plating tools were obtained from ROFIN, BTU, and MECO respectively. Screen printing tool characteristics were taken from [RIC13]. For all tools, the floor space accounts for both tool

footprint and service space and hence is defined as: (tool length+4 m) x (tool width+3 m). As steps are inter-dependent, the throughput rate at capacity (wfr/h) of a particular step is defined by the ratio between its productive time (h/year) and the amount of wafers coming out of the previous step (wfr./y). Thus, calculations are capped by the throughput of the previous step (~2500 wfr/h) and not by the nominal throughput listed by tool suppliers which is higher than this number. The productive time is obtained from the difference between the operations time (24h/day, 330 days/y) and the sum of standby time and down time (tool specific). The amount of wafers coming out of a step is then obtained by multiplying the throughput rate at capacity with the productive time and subtracting yield losses (wfr/y) which are tool specific.

Table 10.1. Characteristics of the printing, laser, sintering, and plating tool used in for CoO calculations. Input values for a silver (Ag) screen printer were obtained from [RIC13] while other values were obtained by direct contact with tool manufacturers. The cost of DI water treatment includes investments in a facility to concentrate water and treatment of the resulting sludge in an off-site recycling station. Note that yield losses (wfr/y) are obtained by multiplying the yield with throughput rate at capacity (wfr/h) and the productive time (h/y).

Cost element (Manufacturing in China)	Ag printing (Baccini Pegaso)	Laser (ROFIN)	Sintering (BTU)	HF/Ni/Cu/Ag plating (MECO)	HF/Ni/Sn plating (MECO)	unit
Listed/estimated price	750,000	1,100,000	350,000	2,200,000	1,400,000	€
floor space (200€/m^2/y)	35.4	50	93	150	70	m^2
yield	0.995	0.999	0.999	0.998	0.998	
Power consumption (0.05eur/kWh)	6	10	70	200	90	kW
Compressed air (0.005€/m^3)	15	72		2	2	m^3/h
N_2 (0.20€/m^3)			15			m^3/h
Cooling water (0.34€/m^3)			1.4			m^3/h
DI water (3.4€/m^3)				1.3	0.8	m^3/h
Vacuum (0.005€/m^3)	30.96					m^3/h
Exhaust air (0.00025€/m^3)	864	250	154	4000	3000	m^3/h
DI water treatment (9.6€/m^3)				1.3	0.8	m^3/h

Utilities and waste disposals mostly impact plating costs. As compared to electroless plating tools, electrolytic plating tools (LIP and electroplating) now provide high plating rates and stable baths which can operate for much longer periods of time since consumed metal ions are being replaced by dissolution of metal anodes. Though this reduces the cost of treating metal contaminated solutions, electrolyte drag-out and DI rinse water consumption can still result in an non-negligible cost. For electrolytic plating, electricity consumption is partly driven by plated thicknesses and hence its associated cost can be reduced when plating thinner lines (see below).

Materials and consumables are listed in Table 10.2. For SP-Ag it is clear that they are dominated by the cost of silver paste which was assumed at 550€/kg. As demand for Ag is foreseen to increase [VER13], CoO calculations were also performed for 700€/kg and 1000€/kg. For the plating sequence, materials costs are dominated by metal consumption, baths make-up (electrolytes are entirely replaced once a year), and electrolyte drag-out which was taken from [RIC13]. Metal consumption was calculated based on a grid design with 3 busbars (1.5mm wide), 10 µm wide fingers with a pitch of 1mm, and Ni/Cu/Ag thicknesses of 1, 7, and 0.1 µm

respectively. In the second part of this chapter, calculations were performed for Ni/Sn thicknesses of 1 and 0.5 µm respectively. Costs of Ni, Cu, Ag, and Sn anodes were obtained from MECO while costs of 1.5%HF bath and of plating electrolytes were calculated from the cost paid by imec assuming a 50% discount could be negotiated when buying larger volumes. For a typical Ag electrolyte this brings the cost down to 38€/l which comes close to the 27.5€/l that represent the typical 50g/l of Ag present in the electrolyte (for Ag at 550€/kg).

Table 10.2. Materials and consumables for printing and plating (MECO plating tool). Metal consumption and bath volumes are calculated for a specific grid design (details in text) and assuming Ni, Cu, Ag thicknesses of 1, 7, and 0.1 µm respectively. Note that the thin Ag immersion plating can be replaced by Sn plating which is thicker since typically electroplated. Electrolyte consumption is taken from [RIC13].

	cost	unit	consumption	unit
Ag paste	550	€/kg	160	mg/wfr
Front Ag Screen	62	€/piece	3734	pieces/y
Squeegee Blade	5.93	€/piece	678	pieces/y
Ni plating (1µm)	30	€/kg	0.008	mg/wfr
Cu plating (7µm)	10	€/kg	0.058	mg/wfr
Ag plating (0.1µm)	550	€/kg	0.001	mg/wfr
Ni electrolyte (1280l bath)	2.06	€/l	0.003	ml/wfr
Cu electrolyte (2250l bath)	3.45	€/l	0.003	ml/wfr
Ag electrolyte (150l bath) for Ag at: 550/700/1000 €/kg	38/48/60	€/l	0.003	ml/wfr
1.5% HF (150l bath)	0.0336	€/l	0.003	ml/wfr
Sn plating (0.5 µm)	45	€/kg	0.003	mg/wfr
Sn electrolyte (150l bath)	3.09	€/l	0.003	ml/wfr

Inputs used to calculated labors costs are summarized in Table 10.3. It is conservatively assumed that one operator per shift in a five shifts per week regime is needed to run a plating tool, the annual cost for one operator being 15000€ (manufacturing in China). For laser ablation and Ag screen printing, 0.5 operator per shift were assumed. For sintering, supervision was assumed to be sufficient as this is typically done with firing furnace equipment.

Table 10.3. Inputs used to calculated labors costs (manufacturing in China).

step	operator/shift (15000€/y.)	supervision/shift (18000€/y.)	engineering (30000€/y.)	maintenance (15€/hrs.)
Ag screen printing	0.5	0.07	0.13	200 hrs./y
Laser	0.5	0.07	0.13	100 hrs./y
Plating	1	0.07	0.13	200 hrs./y
Sintering	0	0.07	0.13	175 hrs./y

10.3. Cost of ownership

10.3.1. Ni/Cu/Ag plated front contacts

The calculated front metallization costs for front laser ablation, Ni/Cu/Ag plating, and N_2 belt furnace sintering are given in Figure 10.1a. For all three steps, depreciation represents the largest share of total costs per cell. This is followed for plating by the costs associated with DI water treatment (i.e. waste disposal) of metal contaminated water even though electrolyte drag-out (~0.003 ml/wfr) and DI water consumption (1.3 m^3/h) are relatively low for the MECO tool due to its cascade rinsing process. Note that the cost associated with DI water treatment would more than triple for a tool with an important electrolyte drag-out of 0.5 ml/wfr as listed in [RIC13]. An important electrolyte drag-out would also impact materials and consumables as plating electrolytes need to be replaced (or spiked) on a more regular basis. Therefore, both electrolyte drag-out and DI-water consumption are parameters that should be looked at when selecting a plating tool. Electricity consumption and nitrogen consumption (required to maintain an oxygen free atmosphere) also play an important role for plating and sintering respectively.

The motivation to reduce Ag consumption is evident from the results given in Figure 10.1b. Materials and consumables, which also include screens and squeegee blades, represent about 80% of total costs associated with screen printing 160 mg of Ag per wafer (typical value for industry [ITR13]). Materials and consumables costs can be reduced by implementing laser ablation, Ni/Cu/Ag plating, and sintering which altogether come out ~4.4€c/cell cheaper than printing 160 mg of Ag per wafer. Though cutting Ag usage down to 80 mg/cell has recently been demonstrated [MUS13] and appears to be yield a similar cost reduction, it should be mentioned that we assumed identical yield losses and screen costs (cost per screen, replacement frequency) which might not be the case when implementing such technology in production.

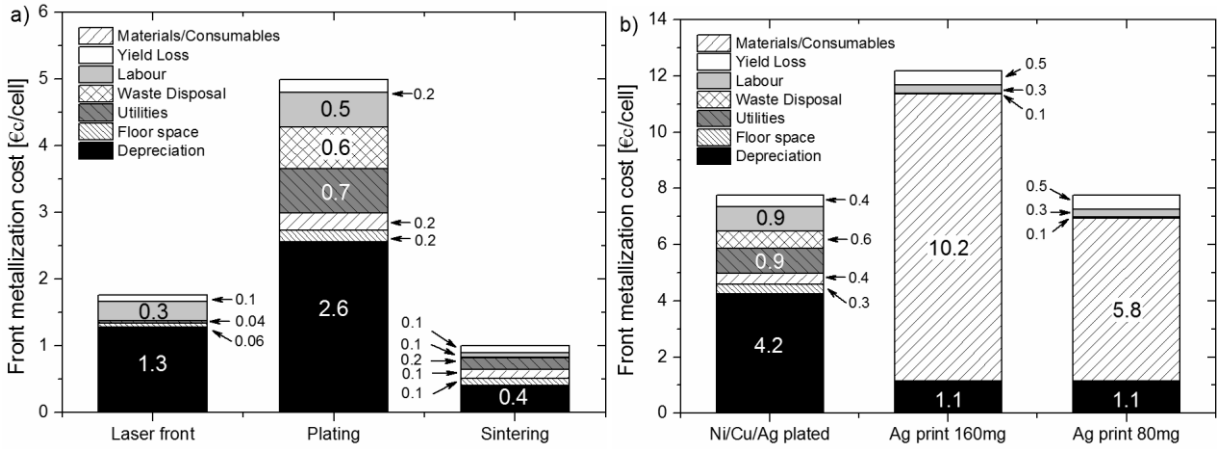


Figure 10.1: a) Front metallization costs breakdown of laser ablation, Ni/Cu/Ag plating (1/7/0.1 µm respectively), and N_2 sintering in a belt furnace. b) Front metallization cost breakdown for Ni/Cu/Ag plated contacts (laser + plating + sintering) as compared to conventional screen printed Ag contacts using 80 mg or 160 mg of Ag per cell.

Despite efforts to reduce Ag consumption for front contacting in the last four or five years, this cost element has not generally been reduced in production owing to a doubling of the average yearly Ag price between 2008 and 2012 (see Figure 10.2a). Though Ag prices have returned to their 2010 level (Ag~500-550€/kg), the industrial demand for Ag is foreseen to grow [VER13]. Furthermore, if the PV industry continues its fast growth and Ag remains the dominant metallization method, within a few years PV will be the major user of Ag putting further pressure on Ag prices and speculation around Ag might resume.

Based on the difference between average prices for 156 mm CZ-Si solar cells and wafer prices we estimate the average wafer-to-cell conversion cost at 67€c/cell in October 2013 [PVI13]. Note this assumes that cell manufacturers sell solar cells at manufacturing cost (no margin). For 156 mm semi-square (area: 239 cm^2) CZ-Si solar cells with an efficiency of 19% (i.e. 4.54 Wp), which can be achieved with standard Al-BSF technology, this translates to a wafer-to-cell CoO of 14.75€c/Wp. At a bulk Ag price of 550€/kg, a printing step based on 160 mg of Ag (12.2€c/cell) accounts for ~18.2% of wafer-to-cell conversion costs and all other steps amount to 54.8€c/cell. Using this latter amount, we can re-calculate the wafer-to-cell CoO when replacing the 160 mg of Ag printing step by either Ni/Cu/Ag plated contacts or a printing step based on 80 mg of Ag. At a Ag cost of 550€/kg and assuming such a replacement does not yield higher cell efficiencies nor impact other processing costs, we find a CoO of ~13.78¢€/Wp for Ni/Cu/Ag plated contacts which is identical to one for printing 80 mg of Ag (see Figure 10.2b). Shall the Ag price return to 700€/kg, cells with Ni/Cu/Ag plated front contacts would have an advantage of ~0.26€c/Wp which would require Ag printed cells to deliver ~0.4%$_{abs.}$ higher efficiencies to remain cost-competitive. This is difficult to imagine considering the fact that the best p-type PERC cell at imec with Ag screen printed contacts currently delivers 0.5%$_{abs.}$ lower efficiency than its counterparts with Ni/Cu/Ag plated contacts (~20.7%, see Chapter 5).

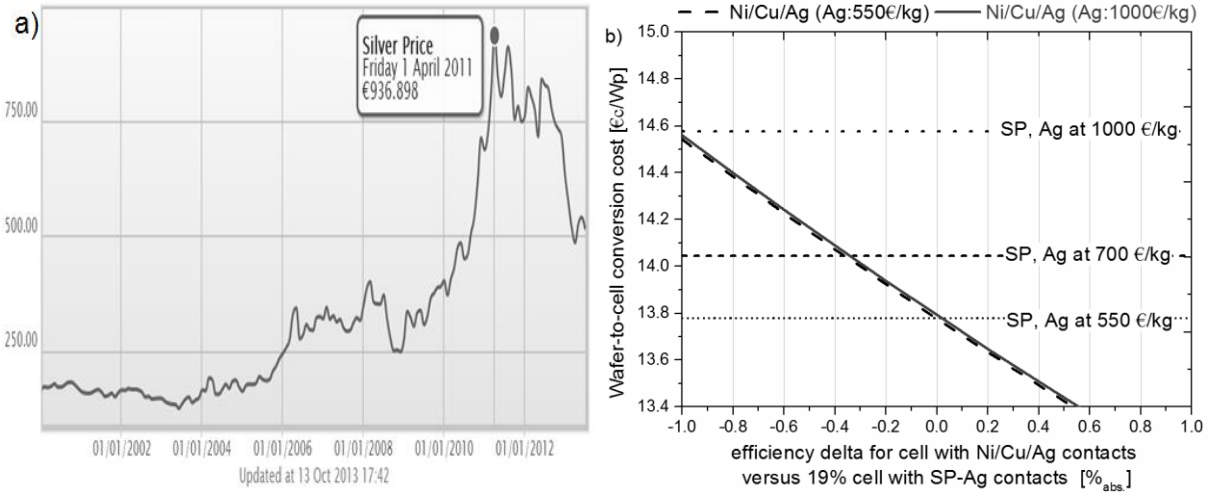


Figure 10.2: a) Silver price in €/kg since 2000 [source: www.bullionbypost.co.uk]. b) Wafer-to-cell conversion costs per Watt peak as a function of efficiency delta between a cell with Ni/Cu/Ag contacts and a 19% 156mm mono CZ-Si cell (i.e. 4.54Wp) featuring screen printed (SP) Ag contacts (80 mg/cell). For both cell structures, non-front metallization costs are identical (54.8 €c/cell) and front metallization costs are recalculated for each Ag price.

10.3.2. Ni/Sn plated front contacts

Due to growing concerns over costs associated with Ag consumption, alternative module manufacturing techniques that are based on 4, 5, 16, or even 30 busbars have (re-)emerged as a way to considerably reduce Ag consumption (see Chapter 3.3). In all cases, the idea is to reduce the finger-to-busbar distance so that finger widths, and hence printed Ag amounts, can be reduced without leading to higher series resistance losses. Numerical simulations have already been performed that indicated that Ag thickness could be reduced down to 2 to 4 µm when employing a mesh of 16 copper wires ("multi-busbar" from Schmid). In addition, using fine-line printing techniques, Ag consumption could potentially be reduced down to 20 to 40 mg per cell with this approach as busbars are no longer needed. Thus, one could wonder what is the added value of replacing such small amounts of printed Ag by the three-step Ni/Cu/Ag plating sequence developed in this thesis. However, in Chapter 4 we performed numerical simulations that revealed that a mesh of 16 copper wires would also be strongly beneficial for Ni/Cu/Ag plated contacts and that the plated thickness could be reduced down to ~1-2 µm. For such low thicknesses, one could imagine to plate only Ni and Ag (capping layer). Note that adhesion data collected in Chapter 7 indicates that thin plated lines may well improve busbar and finger adhesion. Going further, we could imagine skipping the sintering step as we have shown in Chapter 5 that Ni alone enables sufficiently low contact resistance values on moderately doped emitters. Finally, skipping the sintering step would also enable: (i) replacing Ag by Sn (melting point ~230˚C) which is much cheaper, and (ii) using alternative hybrid cell structures with a high efficiency potential as shown in Chapter 9.

It is worth mentioning that we expect many associated costs to decrease when reducing plated thickness. For the MECO inline pilot plating tool installed at imec, replacing Ni/Cu/Ag: 1/7/0.1 µm by Ni/Sn: 1/0.5 µm would reduce electricity consumption (proportional to thickness) and both electrolyte drag-out and DI-water consumption (1 plating bath less). This would result in simpler tool which can either be designed for higher throughput or for being cheaper and smaller. Similarly, eliminating the busbars would reduce the time required for front side ablation by half thus leading again to either a simpler or higher throughput tool. On the contrary, fine line printing of 40 mg would not reduce costs other than Ag consumption and would be likely to result in both higher process complexity and higher yield losses (finger interruptions).

For screen printing, calculations only accounted for a decrease in Ag consumption down to 40 mg per cell (other costs were kept identical) which enables to bring front metallization cost down to ~5.6€c/cell (see Figure 10.2b). This is ~2.2€c/cell cheaper than screen printing 80 mg of Ag per cell which gives some room to introduce the "multi-busbar" technology from Schmid ($Sn_{62}Pb_{36}Ag_2$ coated Cu wires) or the "Smart Wire Contacting Technology (SWCT) from Meyer Burger ($In_{50}Sn_{50}$ coated Cu wires embedded in adhesive). Note that rear Ag soldering pads are no longer required with SWCT reducing costs by another 5€c/cell. Finally, considering the proven efficiency advantage of these two technologies [BRA13, PAP13] would make them even more attractive on a €/Wp basis.

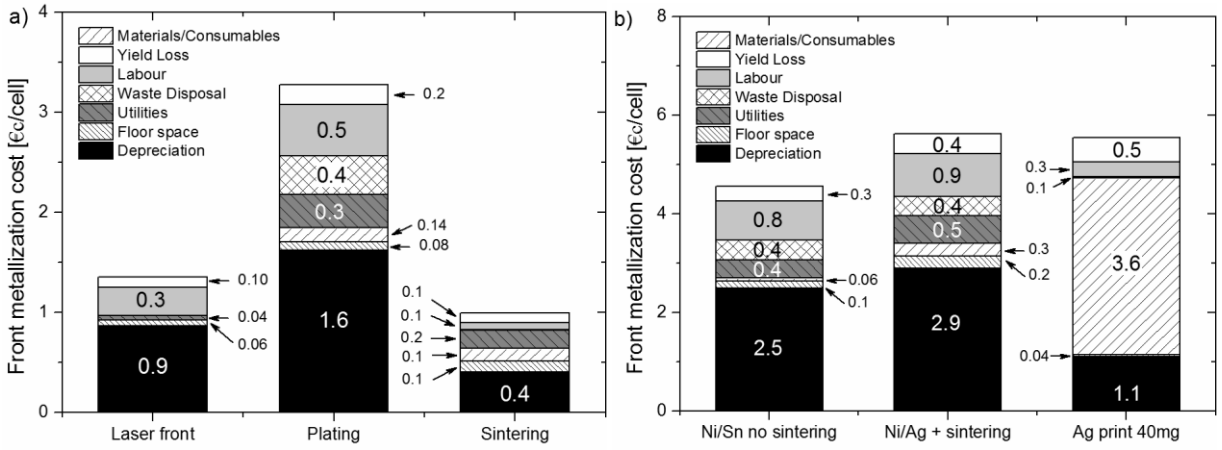


Figure 10.2: a) Front metallization cost breakdown of front laser ablation (no busbar ablation), Ni/Ag plating (1/0.1 µm respectively), and N_2 sintering. b) Front metallization cost breakdown for Ni/Ag plating with sintering and for Ni/Sn (1/0.5 µm respectively) without sintering as compared to screen printing 40mg/cell of Ag (Ag at 550 €/kg).

For the plating sequence, we assumed that plating thin Ni/Sn or Ni/Ag layers would enable the use of a cheaper (1,400,000€) and more compact (70 m^2) plating tool. We also assumed that power consumption would be scaled down to 90 kW based on the difference in plated thicknesses while DI rinse water, and hence DI water treatment, would lower to 0.8 m^3/h (1 plating step less). Finally, skipping ablation of the busbars was accounted for by assuming a cheaper laser tool (750,000€) while keeping its footprint identical. All other costs (labor, etc.) were assumed to be identical. These assumptions led to a front metallization cost of ~5.6€c/cell for sintered Ni/Ag contacts and of 4.5€c/cell for Ni/Sn plating without sintering (Figure 10.2b). Based on these results, we can conclude that thin Ni/Ag plated contacts would remain competitive even against printing as low as 40 mg of Ag per cell (~5.6 €c/cell). This is quite remarkable as we did not consider in the calculations the fact that printing such low amounts might lead to higher process complexity and higher yield losses. Again, the advantage of using thin Ni/Ag plated contacts would become more important shall Ag prices return to a higher level.

10.4. Return on investment

For Ni/Cu/Ag plated front contacts to be economically viable as compared to Ag screen printed contacts, the additional profits generated by reducing wafer-to-cell conversion costs should outweigh the additional investments, or capital expenditures (CAPEX), required for replacing a screen printing system by a trio of systems (laser + plating + sintering). This is evaluated by performing return on investment (ROI) calculations which enable to determine how many years are required for technology A to be more profitable than technology B according to:

$$ROI\ (years) = \frac{CAPEX_{total,A} - CAPEX_{total,B}}{profit_A - profit_B} \quad (10.1)$$

An important element is that the ROI should be well below 5 years as PV systems are typically outdated after such a period of time due to fast technological improvements.

In this chapter, ROI calculations were done on the basis of a single production line making full Al-BSF CZ-Si solar cells. Assuming a constant average selling price (ASP) at 17.7€c/Wp which corresponds to a 20% gross margin for a 19% cell with a wafer-to-cell CoO of 14.75€c/Wp (see section 10.4.1), we evaluated the impact of various front metallization schemes on ROI without taking into considerations additional steps that might be required (e.g. thermal oxidation) when introducing Ni/Cu/Ag plated front contacts. Therefore, the annual profit generated by technology A was simply obtained from:

$$profit = N_{total,A} * P_A * (ASP - CoO_A) \quad (10.2)$$

with $N_{total,A}$ the total number of good cells produced per year (accounts for yield losses), P their average power (in Wp), and CoO the wafer-to-cell conversion cost (€/Wp).

In an effort to assess present and future challenges of plated contacts versus screen printed Ag contacts, ROI calculations were performed using a bulk Ag at 550€/kg (ROI input values given in Table 10.4) or at 700€/kg (ROI input values not shown). Front metallization CAPEX and front metallization cost per cell were taken from Table 10.1 and from Figure 10.1 respectively. Non-front metallization CAPEX (10M€) and non-front metallization costs per cell (54.8€c/cell) were assumed to be identical except for cells specifically designed for Smart Wire Contacting Technology (SWCT). In that case, the following assumptions were made:

- SWCT tool as direct replacement for standard tabber/stringer (no extra CAPEX)
- rear Ag soldering pads no longer needed (non-front metallization CAPEX: 750k€ lower, non-front metallization cost: ~5€c/cell cheaper, higher N_{total} due to lower yield losses)
- higher material cost as compared to standard $Sn_{62}Pb_{36}Ag_2$ coated Cu ribbons since Cu wires are embedded in an adhesive film and coated with $In_{50}Sn_{50}$ to enable low temperature soldering to Al during lamination [PAP13] (non-front metallization cost: 3€c/cell higher)

Table 10.4. Input values used for return on investment (ROI) calculations (details in text) based on Ag at 550€/kg.

	Printed Ag 160 mg/cell	Printed Ag 80 mg/cell	Ni/Cu/Ag +sintering	Ni/Ag +sintering +SWCT	Ni/Sn +SWCT	Printed Ag 40 mg/cell +SWCT	units
non-front metal. CAPEX	10.00	10.00	10.00	9.25	9.25	9.25	[M€]
front metal. CAPEX	0.75	0.75	3.65	2.50	2.15	0.75	[M€]
$CAPEX_{total}$	10.75	10.75	13.65	11.75	11.40	10.00	[M€]
non-front metal. cost	54.80	54.80	54.80	52.95	52.95	52.95	[€c/cell]
front metal. cost	12.18	7.76	7.75	5.62	4.56	5.62	[€c/cell]
total cost	66.98	62.56	62.55	58.57	57.51	58.57	[€c/cell]
P: power (area: 243.4 cm^2)	4.54	4.66	4.66	4.66	4.66	4.66	[Wp/cell]
CoO: cost per Wp	14.75	13.42	13.42	12.57	12.34	12.57	[€c/Wp]
ASP: selling price	17.70	17.70	17.70	17.70	17.70	17.70	[€c/Wp]
N_{total} : number cells out	17.10	17.10	17.18	17.22	17.32	17.10	[M/year]

Introducing Ni/Cu/Ag plated front contacts instead of industrial Ag screen printed contacts (160 mg/cell) would return a ROI of about 2.5 years without requiring any efficiency increase (Figure 10.3a). This result demonstrates that the simplified plating sequence (laser ablation + plating + sintering) developed in this thesis would be economically viable against industrial Ag screen printed contacts if no additional steps (e.g. thermal oxidation) are needed.

Future improvements in printing technology enabling to print only 80 mg/cell without any additional CAPEX or yield losses (as compared to conventional printing) would drastically increase the ROI of Ni/Cu/Ag plated contacts (see Figure 10.3b). Because of the higher CAPEX needed, cells with Ni/Cu/Ag plated contacts should deliver 1%$_{abs.}$ higher efficiencies than their counterparts with Ag contacts (80 mg/cell) in order to maintain a ROI below 2.5 years.

A more attractive solution is to introduce thin Ni/Ag (or Ni/Sn) plated contacts in combination with SWCT since this would result in a ROI below 1 year even when compared against a Ag printing step of 80 mg/cell. Although the use of SWCT possibly enables to reduce Ag consumption further down to 40 mg/cell, we find that a ROI ~2.5 years would still be achievable with Ni/Sn contacts provided the sintering step can be skipped (see Figure 10.3c).

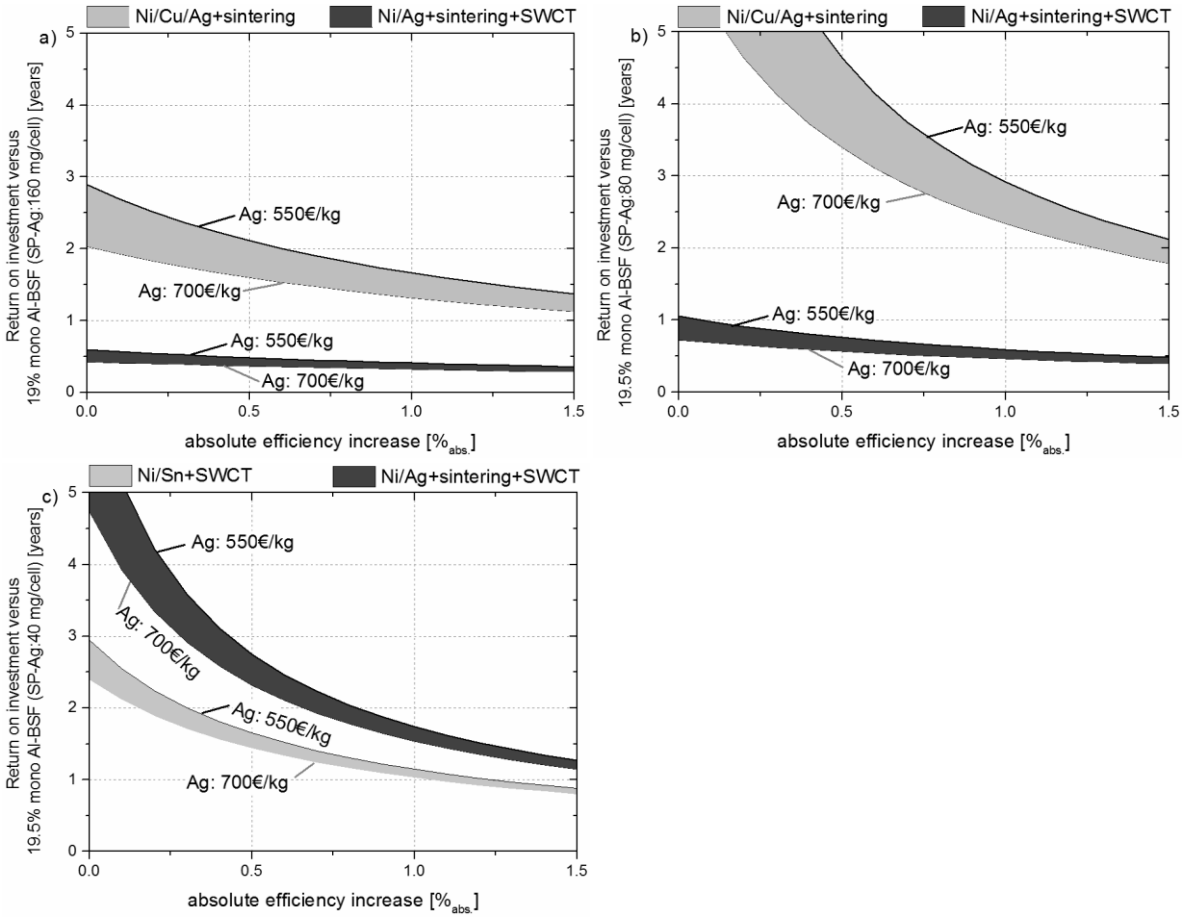


Figure 10.3: a) Return on investment (ROI) for cells with Ni/Cu/Ag (or Ni/Sn) front contacts versus 19% mono Al-BSF cells with screen printed (SP) Ag front contacts (160 mg/cell). b) ROI for cells with Ni/Cu/Ag (or Ni/Sn) front contacts versus 19.5% mono Al-BSF cells with SP-Ag front contacts (80 mg/cell). c) ROI for cells with Ni/Sn front contacts, with and without RTA, versus 19.5% mono Al-BSF cells with SP-Ag front contacts (40 mg/cell).

10.5. Chapter summary

The approach taken in this chapter was to calculate the front metallization cost of the simplified plating sequence developed in this thesis (laser ablation+ plating + sintering) and compare it to one for screen printed Ag contacts. Although such an approach does not account for extra processing steps (e.g. thermal oxidation) that might be required when using plated contacts, it presents the advantage of not assuming any efficiency advantage. Direct comparison is done on a €/cell basis and the cost advantage of plated contacts can be demonstrated shall other processing steps remain the same. Most important results are summarized in Table 10.5.

Table 10.5. Summary of front metallization cost per cell for screen printed (SP) Ag contacts or plated contacts.

Technology type:	this work	standard SP	advanced SP	fingers only	fingers only
Ag price [€/kg]	Ni/Cu/Ag [€c/cell]	Ag: 160 mg/cell [€c/cell]	Ag: 80 mg/cell [€c/cell]	Ag: 40 mg/cell [€c/cell]	Ni/Sn (no sintering) [€c/cell]
550	7.8	12.2	7.8	5.6	4.6
700	7.8	14.6	9.0	6.2	4.6

Calculations were first performed for a simplified plating sequence based on Ni/Cu/Ag plated front contacts and results compared to screen printed Ag contacts. At a Ag price of 550€/kg, we found that replacing Ag screen printing front contacts (160 mg/cell) by Ni/Cu/Ag plated contacts would reduce front metallization wafer-to-cell conversions costs by ~4.4€c/cell (~6.8€c/cell for Ag at 700€/kg). It was then shown that doing such a replacement would give a return on investment (ROI) of about 3 years (2 years for Ag at 700€/kg) which demonstrates that the plating sequence developed in this thesis can be economically viable even without any efficiency increase. However, we also pointed out that future developments in screen printing allowing a reduction in Ag consumption down to 80 mg/cell without additional CAPEX or yield losses would drastically increase the ROI of Ni/Cu/Ag plated contacts.

Finally, we brought attention on the fact that novel interconnections techniques (multi-busbars, SWCT) would strongly benefit to thin plated front contacts since, unlike with fine-line printing, both process complexity and CAPEX would decrease significantly (no busbar ablation, faster/cheaper plating). In addition, techniques such as SCWT would no longer require rear Ag soldering pads thereby enabling additional reductions in both CAPEX and processing costs. Provided that the sintering step could be skipped, we found that thin Ni/Sn (1/0.5 µm respectively) plated contacts would remain cost-competitive against printing as low as 40 mg of Ag per cell with a ROI ~2.5years even without any efficiency increase. Compatibility tests between thin plated layers and novel interconnections techniques have already been started by other research groups with promising results [EDW13]. Thus, this would be an interesting topic for future research particularly when combining it with hybrid cell structures that would benefit strongly from reduced recombination under the front (passivated) busbars (see Chapter 9).

CHAPTER 11

Conclusions and outlook

The work presented is this thesis has been devoted to the development of nickel/copper (Ni/Cu) plated contacts as an alternative to silver (Ag) screen-printed (SP) contacts for the front side metallization of industrial high efficiency silicon (Si) solar cells. This work was motivated not only by the limitations that SP-Ag contacts have regarding cell efficiencies (high shading losses, limited line conductivity, and poor contact resistance to moderately doped junctions), but also by the PV industry's desire to reduce Ag usage below 50 mg/cell for cost reasons by 2017.

Numerous seed-and-plate technologies were first reviewed and self-aligned Ni/Cu plated contacts were chosen as being the best candidate. Copper was chosen at it is the second most conductive metal after Ag while being much cheaper. Nickel was chosen because it: (i) is an inexpensive material (unlike platinum or palladium), (ii) can be deposited using electrochemical methods (unlike titanium), (iii) can be used to form nickel silicides contacts with low contact resistance even on moderately doped junctions, and (iv) has been shown to be a sufficient barrier against Cu diffusion. Despite the potential advantages of Ni/Cu contacts, their commercialization has so far been limited, with the notable exception of BP Solar between the years 1992 and 2008. Reasons for the limitation include a number of challenges (increased process complexity, lack of suitable low-cost production techniques/tools at that time, doubts over cost-advantage and long-term reliability) as well as recent progress made with industrial SP-Ag contacts. Thus, it was the objective of this thesis to demonstrate a simple/fast/reliable/cost-competitive process sequence to define Ni/Cu plated front contacts in industrial high efficiency silicon solar cells.

To reduce process complexity, we restricted ourselves to the use of homogeneous emitters and evaluated, in an incremental approach, low-cost techniques enabling a reduction in the number of processing steps. Performing the sintering step required for nickel silicidation directly after the deposition of a thin (40 nm) PVD Ni layer, we first demonstrated equivalent cell results when substituting photolithography (wet etch) patterning of the front dielectric(s) by ns-UV laser ablation. Extensive analysis revealed that low temperature silicidation (Ni_2Si phase) was best to minimize junction damage and that defects generated during ns-UV laser ablation on alkaline textured surfaces could lead to pseudo fill-factor degradation on 450 nm deep junctions even for Ni_2Si thicknesses below 50 nm. Electroless NiP or bias-assisted light-induced plated (LIP) Ni layers were then evaluated as alternatives to PVD Ni. Nickel silicidation kinetics were shown to be slower for alkaline electroless NiP deposits than with PVD Ni and mechanisms were proposed to explain this. In the case of bias-assisted LIP Ni, deposition on Si was described and silicidation at temperatures as low as 250˚C could be achieved. Unlike electroless NiP, bias-assisted LIP Ni was found to offer fast plating rates and stable baths over long periods of time making it suitable for production. Bias-assisted LIP Ni was selected for further process

simplification which consisted in: (i) depositing a thick (~1 µm) Ni layer that served both as contact layer and Cu diffusion barrier, (ii) performing the sintering step at the end of a simple HF/Ni/Cu/Ag sequence, and (iii) using pilot-production plating and sintering tools. Co-optimization of the front emitter profile, front dielectric(s), and front laser ablation parameters was shown to be required when using this simplified sequence not only for solar cell performance but also to ensure sufficient adhesion and long-term reliability. In particular, the use of thermal oxidation (SiO_2/SiN_x front dielectric stack) was found to be beneficial to control junction depth and reduce parasitic plating but was shown to have a negative impact on front reflectance, bulk lifetime, contact resistance, and front laser ablation thresholds.

The simplified sequence developed in this thesis uses industrial plating techniques and tools that were not available to earlier Ni/Cu adopters like BP Solar, providing more robust and cheaper processing than previously possible. High average cell efficiencies ~20.5% (109 cells) with a top efficiency of 20.7% (externally confirmed at ISE-Callab) and with a tight distribution were demonstrated when applying this sequence to 156x156 mm^2 p-type PERC cells which shows a repeatable and robust metallization process sequence. To the best knowledge of the author, only Schott Solar is currently reporting externally confirmed efficiencies on large area p-type CZ-Si solar cells higher than this (21.3%, [MET13]). First modules made from similar cells passed 1.5x thermal cycling and damp heat testing as defined in IEC61215 and accelerated thermal ageing tests indicated that long-term reliability (25+ years at 85˚C) is feasible. While not enough to fully demonstrate the long-term reliability of Ni/Cu/Ag plated contacts yet, it is a good starting point, with further testing planned. Considering front metallization costs only, higher capital expenses were estimated when replacing a Ag printer by a trio of systems (laser ablation, plating, and sintering). Nevertheless, at a Ag price of 550€/kg, we found that replacing Ag screen printed front contacts (160 mg/cell) by Ni/Cu/Ag plated contacts would reduce front metallization wafer-to-cell conversions costs by ~4.4€c/cell (~6.8€c/cell for Ag at 700€/kg). We also found that doing such a replacement would give a return on investment of about 3 years (2 years for Ag at 700€/kg) which demonstrates that the plating sequence developed in this thesis can be economically viable even without any efficiency increase.

The simplified sequence to define Ni/Cu/Ag plated front contacts was then evaluated for the first time in rear junction n-PERT cells as it may enable to: (i) benefit from higher bulk-lifetime without suffering from light-induced degradation present in p-type CZ-Si, (ii) minimize the impact of front ablation and/or silicidation on junction damage, and (iii) maximize long-term reliability since accelerated thermal ageing tests on p-PERC cells revealed that deeper junctions were preferred. Efficiencies up to 20.5% with encouraging V_{oc}~674±2mV were obtained on 156x156 mm^2 cells in a first trial. Finally, a power-loss analysis was conducted which confirmed the higher efficiency potential of n-PERT and its stronger tolerance to thin wafers (lower cost).

In parallel, excimer laser annealing (ELA) was evaluated extensively as we could demonstrate improved control of nickel silicide formation with this technique. However, ELA introduces extra complexity/costs which could not be justified in p-PERC cells as results on 0.3 µm deep junctions (potentially cheaper to manufacture) were limited by junction damage created

during laser ablation of the front dielectric(s) and not by the silicidation method. Nevertheless, we could show that ELA is a one-side heating process by making hybrid n-PERT cells based on heterojunction rear emitter which resulted in efficiencies up 20.2% with $j_{0,rear}$~10 fA/cm^2 on textured surfaces. This result is promising as it offers to combine a simple 1D design and good surface passivation at the rear side with the advantages listed above for rear junction n-PERT.

Future work should aim at eliminating concerns over reliability and cost-advantage of Ni/Cu/Ag plated contacts without compromising on simplicity and high-throughput processing.

One aspect that requires further in-depth investigations is the influence of defects generated during laser ablation of front dielectrics on both I-V results and reliability results. As mentioned in Chapter 5, laser-induced defects may serve as paths, during silicidation, for Ni diffusion and subsequent Ni clustering in the space charged region thereby explaining the measured lower pFF values as compared to samples patterned by wet etching. Therefore, it would be interesting in the future to correlate I-V and reliability results to laser-generated defect density and depth. Similarly, ns-UV and ps-UV laser pulses should be compared again but this time using identical optics, which was not possible in this work. Finally, the ability to perform pulse shaping (e.g. top-hat profiles, asymmetrical pulses, etc.) deserves further attention as it could help improving ablation uniformity as well as processing speeds.

Another aspect that was touched upon in this thesis and that should be further explored is the ability to engineer plating deposits properties as to maximize adhesion results. In addition, implementing low-cost HF-free chemistries for native oxide removal prior to Ni plating should also be explored as it is of particular importance for cost and safety reasons. Similarly, new high-speed plating electrolytes should be investigated as they could enable the design of cheaper, more compact plating tools. As mentioned in Chapter 7, further investigations are required to accurately measure internal stress values and correlate them to both pull tab adhesion results and environmental module testing (thermal cycling, etc.) results. Evaluating the impact of replacing hand-soldering by state-of-the art soldering equipment on adhesion/environmental module testing results could also be considered for future work.

The Ni/Cu metallization expertise that was built-up during this thesis is now being applied to rear junction n-PERT devices as we could show that they present a higher efficiency potential. This will require (again) to reduce process complexity, demonstrate the €/Wp advantage, and build confidence in reliability. Finally, considering novel interconnection techniques that potentially offer to reduce Ag consumption down to 40 mg/cell, we found that using thin Ni/Sn plated front contacts instead of printed Ag contacts would result in a return on investment of about 2.5years even without any efficiency increase. Based on the work presented in this thesis, doing so would greatly reduce front shading losses and be particularly suited for hybrid n-PERT cells. In addition, both process complexity and associated costs can be expected to decrease when moving to thin plated contacts which make it an attractive route to pursue. As a final word, even if considerable efforts are being made in screen printing to reduce Ag usage per cell, we believe that it is only postponing the inevitable switch to Ni/Cu plated contacts especially since Ag prices are likely to rise in years to come due to strong industrial demand.

List of publications

Articles in peer reviewed Journals:

L. Tous, JF. Lerat, T. Emeraud, R. Negru, K. Huet, A. Uruena, M. Aleman, J. Meersschaut, H. Bender, R. Russell, J. John, J. Poortmans, and R. Mertens. *Nickel silicide contacts formed by excimer laser annealing for high efficiency solar cells*. Progress in Photovoltaics: Research and Applications (2013), doi: 10.1002/pip.2362

L. Tous, M. Aleman, R. Russell, E. Cornagliotti, P. Choulat, A. Uruena, S. Singh, J. John, F. Duerinckx, J. Poortmans, and R. Mertens. *Evaluation of advanced p-PERL and n-PERT large area silicon solar cells with 20.5% energy conversion efficiencies,* accepted in Progress in Photovoltaics: Research and Applications

L. Tous, R. Russell, M. Debucquoy, N. Posthuma, F. Duerinckx, R Mertens, J. Poortmans. *Power-loss analysis of advanced PERC cells reaching 20.5% energy conversion efficiency*. Energy Procedia 38 (2013): 467-473. Poster presentation at 3rd Silicon PV conference, Hamelin, Germany, (2013)

L. Tous, R. Russell, J. Das, R. Labie, M. Ngamo, J. Horzel, H. Philipsen, J. Sniekers, K. Vandermissen, L. van den Brekel, T. Janssens, M. Aleman, D.H. van Dorp, J. Poortmans, R. Mertens. *Large area copper plated silicon solar cell exceeding 19.5% efficiency*. Energy Procedia, 21 (2012): 58-65. Oral presentation at 3rd workshop on metallization for crystalline silicon solar cells, Charleroi, Belgium, (2012)

L. Tous, D. H. van Dorp, R. Russell, J. Das, M. Aleman, H. Bender, J. Meersschaut, K. Opsomer, J. Poortmans, R. Mertens. *Electroless nickel deposition and silicide formation for advanced front side metallization of industrial silicon solar cells*. Energy Procedia 21 (2012): 39-46. Oral presentation at 3rd workshop on metallization for crystalline silicon solar cells, Charleroi, Belgium, (2012)

L. Tous, JF. Lerat, T. Emeraud, R. Negru, K. Huet, A. Uruena, M. Aleman. R. Russell, J. John, J. Poortmans, and R. Mertens. *Nickel silicide formation using excimer laser annealing.* Energy Procedia 27 (2012): 503-509. Oral presentation at 2nd Silicon PV conference, Leuven, Belgium, (2012)

A. Uruena, L. Tous, F. Duerinckx, I. Kuzma-Filipek, E. Cornagliotti, J. John, R. Mertens, and J. Poortmans. *Understanding the mechanisms of rear reflectance losses in PERC type silicon solar cells*. Energy Procedia 38 (2013): 801-806. Oral presentation by first author at 3rd Silicon PV conference, Hamelin, Germany, (2013)

K. Van Wichelen, L. Tous, A. Tiefenauer, C. Allebé, T. Janssens, P. Choulat, J.L. Hernandez, E. Cornagliotti, M. Debucquoy, A. Ruocco, J. John, P. Verlinden, F. Dross, K. Baert, *Towards 20.5% efficiency PERC Cells by improved understanding through simulation*, Energy Procedia, 8 (2011): 78–81. Poster presentation at 1st Silicon PV conference, Freiburg, Germany, (2011)

B. Vermang, H. Goverde, L. Tous, A. Lorenz, P. Choulat, J Horzel, J. John, J. Poortmans, R. Mertens, *Approach for Al_2O_3 rear surface passivation of industrial p-type Si PERC above 19%*, Progress in Photovoltaics: Research and applications, (2012), doi: 10.1002/pip.2196

E. Cornagliotti, M. Ngamo, L. Tous, R. Russell, J. Horzel, D. Hendrickx, B. Douhard, V. Prajapati, T. Janssens, and J. Poortmans. *Integration of inline single-side wet emitter etch in PERC cell manufacturing*. Energy Procedia 27 (2012): 624-630. Oral presentation by first author at 2nd Silicon PV conference, Leuven, Belgium, (2012)

R. De Rose, K. Van Wichelen, L. Tous, J. Das, F. Dross, C. Fiegna, M. Lanuzza, E. Sangiorgi, A. Urueña, M. Zanuccolia, *Optimization of Rear Point Contact Geometry by Means of 3-D Numerical Simulation*, Energy Procedia, 27 (2012): 197-202. Poster presentation at 2nd Silicon PV conference, Leuven, Belgium, (2012)

J. John, V. Prajapati, B. Vermang, A. Lorenz, C. Allebé, A. Rothschild, L. Tous, A. Uruena, K. Baert, and J. Poortmans. *Evolutionary process development towards next generation crystalline silicon solar cells : a semiconductor process toolbox application.* EPJ Photovoltaics 3 (2012): 35005.

Contributions to international conferences

L. Tous, R. Russell, J. Beckers, J. Bertens, E. Cornagliotti, P. Choulat, J. John, F. Duerinckx, J. Szlufcik, J. Poortmans and R. Mertens. *A simple copper based plating process resulting in efficiencies above 20.5% using pilot processing equipment*. in Proceedings of the 28th EUPVSEC, Paris, France, (2013). Oral presentation

L. Tous, J-F Lerat, T. Emeraud, R. Negru, K. Huet, R. Russell, J. John, J. Poortmans, and R. Mertens. *Progress in nickel silicide formation using excimer laser thermal annealing*, in Proceedings of the 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, (2012). 691 – 695. Oral presentation.

L. Tous, D.H. van Dorp, J.L. Hernandez, C. Allebé, M. Ngamo, H. Bender, J Meersschaut, M. Aleman, R. Russell, J. Poortmans and R. Mertens, *Minimizing junction damage associated with nickel silicide formation for the front side metallization of silicon solar cells*. in Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, (2011): 1210 – 1215. Oral presentation.

L. Tous, M. Recaman-Payo, M. Ngamo, J.L. Hernández, J. Poortmans, and R. Mertens. *Evaluating contact resistance using epitaxially grown phosphorous emitters*. in Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, (2011): 1413 – 1417. Poster presentation.

M. Aleman, L. Tous, E. Cornagliotti, F. Duerinckx, J. John, N.E. Posthuma, R. Russell, S. Singh, E. Sleeckx, A. Uruena, J. Szlufcik. *Large area high efficiency n-type Si rear junction cells featuring laser ablation and Cu plated front contacts*, in Proceedings of the 28th EUPVSEC, Paris, France, (2013). Oral presentation by first author.

E. Cornagliotti, L. Tous, A. Uruena, A. Rothschild, R. Russell, V. Lu, S. Radosavjlevic, J. John, J. Toman, M. Aleman, F. Duerinckx, J. Poortmans, J. Szlufcik, B. Dielissen, F. Souren, X. Gay, R. Görtzen, B. Hallam. Integration of spatial ALD aluminum oxide for rear passivation of p-type PERC/PERL solar cells, in Proceedings of the 28th EUPVSEC, Paris, France, (2013). Oral presentation by first author.

M. Ngamo, L. Tous, E. Cornagliotti, J. Horzel, T. Janssens, R. Russell, B. Lombardet, J. Poortmans, *Integration of high sheet resistance front homogeneous emitter in a process flow for PERL type cells with Cu contacts*, in Proceedings of the 37th IEEE Photovoltaic Specialists Conference, Austin, USA (2012): 3371 – 3376. Oral presentation by first author

J.F. Lerat, L. Tous, T. Emeraud, R. Negru, K. Huet, J. John, J. Poortmans, and R. Mertens, *Progress in nickel silicide formation using excimer laser annealing: a simulation study*, in Proceedings of the 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, (2012). Poster presentation by first author.

R. Russell, L. Tous, H. Philipsen, J. Horzel, E. Cornagliotti, M. Ngamo, P. Choulat, J. John, J. Poortmans and R. Mertens, *A simple copper metallization process for high cell efficiencies and reliable modules*, in Proceedings of the 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, (2012): 538 – 543. Plenary presentation by first author.

J. Horzel, L. Tous, A. Uruena, A. Seidl, R. Russell, E. Cornagliotti. *CZ-Si material influence on PERL-type Si solar cells*, in Proceedings of the 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, (2012): 780 – 788. Oral presentation by first author.

C. Allebé, L. Tous, K. Van Wichelen, JL. Hernández, M. Aleman, M. Ngamo, J. Poortmans, R. Mertens, *Large area PERC cells with a Ti-Cu based metallization leading to efficiencies above 19.5%*. in Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, (2011): 2276 – 2279. Poster presentation by first author.

J. Das, L. Tous, J.L. Hernández, P. Jaffrennou, M. Ngamo, J. John, N.E. Posthuma, K. Baert, J. Poortmans. *Laser ablation: towards advanced industrial solar cell metallization processes*. in Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, (2011): 1691 – 1693. Poster presentation by first author.

J.L. Hernández, L. Tous, C. Allebé, H. Philipsen, E. Schlenker, J. John, K. Baert, J. Poortmans. *Applications of CMOS metal barriers to copper plated silicon solar cells*, in Proceedings of the 25th European and 5th World Photovoltaic Solar Energy Conference, Valencia, Spain, (2010): 1479 – 1483. Oral presentation by first author.

C. Allebé, L. Tous, B. Vermang, T. Janssens, P. Choulat, J. John, N.E. Posthuma, E. van Kerschaver. *An integrated approach for selective emitter formation*. in Proceedings of the 24th European Photovoltaic Solar Energy Conference, Hamburg, Germany, (2009): 1820 – 1822. Poster presentation by first author.
JL. Hernandez, C. Allebé, L. Tous, J. John, J. Poortmans. *Laser ablation and contact formation for Cu-plated large area c-Si industrial solar cells*. in Proceedings of the 35th IEEE Photovoltaic Specialists Conference, Honolulu, USA, (2010): 3158 – 3162. Oral presentation by first author.

A. Urueña, JF. Lerat, T. Emeraud, L. Tous, F. Duerinckx, J. John, J. Poortmans, R. Mertens. *Excimer laser annealing for boron implanted local BSF for PERC crystalline silicon solar cells*, in Proceedings of the 28th EUPVSEC, Paris, France, (2013). Poster presentation by first author.

P. Choulat, V. Prajapati, E. Sleeckx, S. Singh, L. Tous, B. O'Sullivan, V. Ferro, F. Duerinckx. *Cost effective dry oxidation for emitter passivation: a key step for high efficiency screen printed p-type PERC solar cells*. in Proceedings of the 28th EUPVSEC, Paris, France, (2013). Oral presentation by first author.

E. Cornagliotti, A. Uruena, J. Horzel, J. John, L. Tous, D. Hendrickx, V. Prajapati, S. Singh, R. Hoyer, F. Delahaye, K. Weise, D. Queißer, H. Nussbaumer, J. Poortmans, *How Much Rear Side Polishing Is Required? A Study on the Impact of Rear Side Polishing in PERC Solar Cells.* in Proceedings of the 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, (2012): 561 – 566. Oral presentation by first author.

R. Labie, JL. Hernandez, J. Govaerts, C. Allebé, L. Tous, A. Urueña, R. Russell, I. Gordon and K. Baert. *Cu plated i-PERL cells: ageing and humidity reliability tests.* in Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, (2011): 1195 – 1198. Oral presentation by first author.

C. Allebé, E. Schlenker, J.L. Hernández, M. Aleman, L. Tous, V. Prajapati, K. Van Nieuwenhuysen, T. Janssens, Aude Rothschild, B. Vermang, A. Lorenz, A. Urueña, E. Rosseel, J. John. K. Baert, J. Poortmans, *Process integration towards PERL structure*. in Proceedings of the 25th European and 5th World Photovoltaic Solar Energy Conference, Valencia, Spain, (2010): 1469 – 1474 . Oral presentation by first author.

J. Horzel, P. Choulat, E. Cornagliotti, T. Janssens, J. John, I. Kuzma-Filipek, V. Prajapati, A. Rothschild, R. Russell, S. Singh, E. Sleeckx, L. Tous, A. Urueña, B. Vermang, *Overview on recent improvement for industrially applicable PERL-type Si solar cell processing*. in Proceedings of the 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, (2012): 1602 – 1606. Poster presentation by first author

Other publications:

R. Russell, L. Tous, R. Labie, M. Aleman, F. Duerinckx, J. Bertens, T. Horiuchi. J. Szlufcik. *Cost-effective and reliable Ni/Cu plating for p- and n-type PERx silicon solar cells yielding efficiencies above 20.5%*. Photovoltaics International 21, (2013): 62-69.

Patents:

L. Tous, M. Aleman, J. John, Thierry Emeraud, *Method for forming metal silicides layers*, WO2013076267 A1

G.D.S. Beaucarne, J. Horzel, N.E. Powell, L. Tous, D. A. Wood, A.P. Zambova, *Photovoltaic cell and method of forming the same*, WO2013090562 A2

L. Tous, R. Russell, *Method for improving the adhesion of plated metal layers to silicon*. US provisional

B. Vermang, L. Tous, F. Duerinckx, *Improved front surface passivation*, US Provisional

Bibliography

[ABB06]: Abbott, M. D., J. E. Cotter, T. Trupke, et al. "Investigation of edge recombination effects in silicon solar cell structures using photoluminescence." *Applied physics letters* **88**, no. 11 (2006): 114105-114105.

[ABE11]: Aberle AG, Zhang W, Hoex B, Energy Procedia, "Advanced loss analysis method for silicon wafer solar cells". *Energy Procedia* **8**; (2011): 244-249

[ABE12]: A.G. Aberle, M. B. Boreland, B. Hoex and T. Mueller, "Review Industrial Silicon Wafer Solar Cells – Status and Trends", *Green*; **2**(4); (2012): 135–148

[ABR94]: L.M. Abrantes, and J. P. Correia. "On the Mechanism of Electroless Ni-P Plating." *Journal of the electrochemical society* **141**, no. 9 (1994): 2356-2360.

[ADA07]: B.Adams, D. Jennings, K. Ma, A. J. Mayur, S. Moffatt, S. G. Nagy, and V. Parihar. "Characterization of Nickel Silicides Produced by Millisecond Anneals." *In Proceedings of the 15th IEEE Conference on Advanced Thermal Processing of Semiconductors*, (2007):155-160

[AGO05]: G. Agostinelli, J. Szlufcick, P. Choulat, G. Beaucarne, "Local contact structures for industrial PERC-type solar cells", *In Proceedings of the 20th EUPVSEC*, (2005): 942–945

[ALE09]: M. Aleman, N. Bay, D. Barucha, A. Knorz, D. Biro, R. Preu, S.W. Glunz. "Advances in electroless nickel plating for the metallization of silicon solar cells using different structuring techniques for the ARC." *In Proceedings of the 24th EPVSEC*, (2009): 1414-1418.

[ALE13]: M. Aleman Martinez, "Low temperature processes for the front-side metallization of silicon solar cells", *PhD thesis*, Freiburg (2013).

[ALT00]: P.P. Altermatt, J.O. Schumacher, A. Cuevas, S.W. Glunz, R.R. King, G. Heiser, and A. Schenk. "The extraction of the surface recombination velocity of Si: P emitters using advanced silicon models." *In Proceedings of the 16th EUPVSEC*. (2000).

[AND99]: PC. Andricacos. "Copper On-Chip Interconnections: A Breakthrough in Electrodeposition to Make Better Chips", *The Electrochemical Society Interface*, (1999).

[ARN13]: R. Arndt and R. Puto "Basic Understanding of IEC Standard Testing For Photovoltaic Panels", tuvamerica.com/services/photovoltaics/ArticleBasicUnderstandingPV.pdf, Retrieved 22 October 2013

[BAL13]: C. Ballif, N. Badel, L. Barraud, B. Demaurex, et al. "High-Efficiency Crystalline Silicon Cells Based on Heterojunction Contacts: Improving Optical Performances and Lowering Metallisation Costs", *In Proceedings of the 28th EUPVSEC*, Paris, France (2013).

[BAL13]: T. Ballman, "Transfer of the 20plus high efficiency cell structure into pilot line production", *In Proceedings of the 20plus Workshop*, Chambery, (2013).

[BAR01]: A.J. Bard and L.R. Faulkner, "Electrochemical Methods, Fundamentals and Applications", John Wiley & Sons, New York, 2nd edition, (2001).

[BAR10]: J. Bartsch, A. Mondon, K. Bayer, C. Schetter, et al. "Quick Determination of Copper-Metallization Long-Term Impact on Silicon Solar Cells", *Journal of The Electrochemical Society*, **157**(10); (2010): 942-946

[BAR12]: J. Bartsch, "Advanced Front Side Metallization for Crystalline Silicon Solar Cells with Electrochemical Techniques", *PhD thesis*, Freiburg (2007).

[BAR96]: C.J. Barbero, C. Deng, T. W. Sigmon, S. W. Russell, and T. L. Alford. "The fabrication of nickel and chromium silicide using an XeCl excimer laser." *Journal of crystal growth* **165**, no. 1 (1996): 57-60.

[BAS05]: D. Basting, and G. Marowsky, Excimer laser technology. Springer, (2005)

[BAS88]: P.A. Basore, D.T. Rover, and A.W. Smith, "PC-1D version 2: enhanced numerical solar cell modeling", *In Proceedings of the 20th IEEE PVSC*, (1988): 389-396

[BEA12]: G. Beaucarne, G. Schubert, J. Hoornstra, J. Horzel and S. W. Glunz, "Summary of the third workshop on metallization for crystalline silicon solar cells", *Energy Procedia* **21**; (2012): 2-13

[BEN06]: A. Bentzen, A. Holt, J. S. Christensen, and B. G. Svensson. "High concentration in-diffusion of phosphorus in Si from a spray-on source", *Journal of Applied Physics* **99**, (2006): 064502

[BER89]: W. Bergholz, M.J. Binns, G.R. Booker, J.C. Hutchison, et al., "A study of oxygen precipitation in silicon using high-resolution transmission electron microscopy, small-angle neutron scattering and infrared absorption", *Philosophical Magazine B* **59** (1989) 499.

[BIR09]: D. Biro, S. Mack, A. Wolf, et al. "Thermal Oxidation as a key technology for high efficiency screen printed industrial silicon solar cells", *In Proceedings of the 34th IEEE PVSC*, (2009): 1594-1599

[BIV10]: M. Bivour, C. Meinhardt, D. Pysch, et al, "N-type silicon solar cells with amorphous/crystalline silicon heterojunction rear emitter." *In Proceedings of the 35th IEEE PVSC*, (2010):1304-1308

[BIV12]: M. Bivour, C. Reichel, M. Hermle, and S.W. Glunz. "Improving the a-Si: H (p) rear emitter contact of n-type silicon solar cells." *Solar Energy Materials and Solar Cells*, **106**, (2012): 11–16

[BLA89]: A.W. Blakers, A. Wang, A.M. Milne, J. Zhao, and M.A. Green. "22.8% efficient silicon solar cell." *Applied Physics Letters* **55**, no. 13 (1989): 1363-1365.

[BLA92]: A.W. Blakers, A. W. "Shading losses of solar-cell metal grids." *Journal of applied physics* **71**, no. 10 (1992): 5237-5241.

[BOR95]: A. Borghesi, B. Pivac, A. Sassella, and A. Stella. "Oxygen precipitation in silicon." *Journal of Applied Physics* **77**, no. 9 (1995): 4169-4244.
[BOU10]: C. Boulord, A. Kaminski, Y. Veschetti, et al. "Comparison of different electrochemical deposits for contact metallization of silicon solar cells." *Materials Science and Engineering B* **165**, no. 1 (2009): 53-56.
[BOW01]: S. Bowden, and A. Rohatgi, "Rapid and Accurate Determination of Series Resistance and Fill Factor Losses in Industrial Silicon Solar Cells," *in Proceedings of the 17th EUPVSEC*, (2001): 1802-1806.
[BRA10]: S. Braun, R. Emre, B. Raabe, and G. Hahn. "Electroless nickel and copper metallization: Contact formation on crystalline silicon and background plating behavior on PECVD silicon SiNx: H layers." *In Proceedings of the 25th EUPVSEC*, (2010): 1892 - 1895
[BRA11]: K. Branker, M. J. M. Pathak, and J. M. Pearce. "A review of solar photovoltaic levelized cost of electricity." *Renewable and Sustainable Energy Reviews* **15**, no. 9, (2011): 4470-4482.
[BRA11b]: S. Braun, A. Zuschlag, B. Raabe, and G. Hahn. "The origin of background plating." *Energy Procedia*, **8,** (2011): 565-570.
[BRA13]: S. Braun, G. Hahn R. Nissler, C. Pönisch, D. Habermann. "Multi-Busbar Solar Cells and Modules: High Efficiencies and Low Silver Consumption", *Energy Procedia*, **38**, (2013): 334–339
[BRU03]: T. Bruton, N. Mason, S. Roberts, O. Nast Hartley, S. Gledhill, et al., "Towards 20% efficient silicon solar cells manufactured at 60 MWp per annum", *In Proceedings of the 3rd WPCEC*, (2003): 899-902
[BUR99]: A.R. Burgers, "How to design optimal metallization patterns for solar cells." *Progress in Photovoltaics Research and Applications* **7**, no. 6 (1999): 457-461.
[CAB11]: E. Cabrera, S. Olibet, D. Rudolph, E. Wefringhaus, et al. "Influence of surface topography defects and their nature on the contact formation in thick film Ag metallization", *In Proceedings of the 3rd Metallization workshop*, Konstanz, Germany (2011).
[CAC13]: A. Cacciato, F. Duerinckx, K. Baert, M. Moors, T. Caremans, G. Leys, K. De Keersmaecker, and J. Szlufcik. "Investigating manufacturing options for industrial PERL-type Si solar cells." *Solar Energy Materials and Solar Cells* **113** (2013): 153-159.
[CAR07]: V. Carron, P. Bessonb F. Pierre "Wet Etching Step Evolution for Selective Removal on Silicide or Germanide Applications", *ECS Transactions*, **11** (2), (2007): 309-320
[CAS12]: P. Saint-Cast, D. Kania, R. Heller, S. Kuehnhold, M. Hofmann, J. Rentsch, and Ralf Preu. "High-temperature stability of c-Si surface passivation by thick PECVD Al2O3 with and without hydrogenated capping layers." *Applied Surface Science* **258**, no. 21 (2012): 8371-8376.
[CHA13]: J. Chase, " BNEF University – renewable energy, CCS, EST", Bloomberg New Energy Finance, http://about.bnef.com/presentations/bnef-university-renewable-energy-ccs-est/, retrieved 22 October 2013.
[CHE09]: Y-W. Chen, Nien-Ting Ho, Jerander Lai, T. C. Tsai, C. C. Huang, et al. "Advances on 32nm NiPt Salicide Process." *In 17th IEEE Conference on advanced thermal processing of semiconductors*, (2009):1-4
[CHO05]: P. Choulat, F. Duerinckx, E. Van Kerschaver, F. Dross, G. Beaucarne. "Minimizing the Dead layer of Industrial Phosphorous Emitters Formed by POC13 Diffusion", *In Proceedings of the 15th PVSC*, (2005).
[CLA85]: W.A.P Claassen, W.G.J.N. Valkenburg, et al.. "Influence of deposition temperature, gas pressure, gas phase composition, and RF frequency on composition and mechanical stress of plasma silicon nitride layers." *Journal of the Electrochemical Society* **132**, no. 4 (1985): 893-898.
[COH83]: S.S. Cohen, "Contact resistance and methods for its determination." *Thin Solid Films* 104, no. 3 (1983): 361-379.
[COL80]: M.G. Coleman, R. A. Pryor, and T. G. Sparks. "A base-metal conductor system for silicon solar cells.", *In Proceedings of the 14th PVSC*, 1; (1980): 793-799
[COM96]: R. G. Compton, and G. HW Sanders. "Electrode potentials".Oxford University Press, (1996).
[COR12]: E. Cornagliotti, M. Ngamo, L. Tous, R. Russell, J. Horzel, et al. "Integration of inline single-side wet emitter etch in PERC cell manufacturing." *Energy Procedia* **27** (2012): 624-630.
[COR13]: E. Cornagliotti, L. Tous, A. Uruena de Castro, et al. "Integration of Spatial ALD Aluminum Oxide for Rear Side Passivation of p-Type PERC/PERL Solar Cells", *In Proceedings of the 28th EUPVSEC*, (2013)
[CRA12]: D. Crafts, D. De Ceuster, O.Schultz-Wittmann, A. Turner, "Fine line metallization of photovoltaic devices by partial lift-off of optical coatings", US8236604 B2, (2012)
[CUE00]: A.Cuevas, and DA Russel, "Co-optimisation of the Emitter Region and the Metal Grid of Silicon Solar Cells", *Progress in Photovoltaics Research and Applications*, **8**, no. 6 (2000): 603-616.
[DAI93]: X.M. Dai,, M. A. Green, and S. R. Wenham. "High efficiency n-silicon solar cells using rear junction structures." *In Proceedings of the 23rd IEEE PVSC* (1993): 153-156.
[DAV13]: K.O Davis, K. Jiang, C. Demberger, H. Zunft, H. Haverkamp, D. Habermann, and WV. Schoenfeld. "Investigation of the Internal Back Reflectance of Rear-Side Dielectric Stacks for c-Si Solar Cells." *IEEE Journal of Photovoltaics* (2013): 1-8.
[DEL04]: F. Delahaye, M. Lohrmann, M. Bauer, et al., "Edge isolation: Innovative inline wet processing ready for industrial production," *In Proceedings of the 19th EUPVSEC*, (2004): 416-418
[DEN97]: F. Deng, R. A. Johnson, P. M. Asbeck, S. S. Lau, W. B. Dubbelday, et al. "Salicidation process using NiSi and its device application." *Journal of applied physics* **81**, no. 12 (1997): 8047-8051.

[DeW12]: S. De Wolf, A. Descoeudres, Z.C. Holman, and C. Ballif. "High-efficiency silicon heterojunction solar cells: A review." *Green* **2**, no. 1 (2012): 7-24.
[diB00]: G.A. Di Bari, "Electrodeposition of nickel." Modern electroplating, 4th edition. Wiley, New York (2000): 139-200.
[DUB11]: C.E. Dubé, B. Tsefrekas, D. Buzby, R. Tavares, W. Zhang, A. Gupta, et al. "High Efficiency Selective Emitter Cells Using Patterned Ion Implantation", *Energy Procedia*, 8, (2011): 706-711.
[DUB90]: C. E. Dubé and R. C. Gonsiorawski, "Improved contact metallization for high efficiency EFG polycrystalline silicon solar cells", *In Proceedings of the 21st IEEE PVSC*, (1990): 624-628
[DUE02]: F. Duerinckx and J. Szlufcik, "Defect passivation of industrial multicrystalline solar cells based on PECVD silicon nitride," *Solar Energy Materials and Solar Cells*, **72**; (2002): 231-246.
[DUH12]: A. Duhin, Y. Sverdlov, I. Torchinsky, et al. "NiSi contact metallization using electroless Ni deposition on Pd-activated self-assembled monolayer (SAM) on p-type Si (100)." *Microelectronic Engineering* **84**, no. 11 (2007): 2506-2510.
[DUR79]: L.F. Durkee "Method of plating by means of light." U.S. Patent 4,144,139, issued March 13, 1979.
[DUR84]: L.J. Durney, "Electroplating engineering handbook, part 1, 4th edition", Chapman and Hall, (1984), 226-262
[DUT12]: S. Duttagupta, F. Ma, et al. "Optimised antireflection coatings using silicon nitride on textured silicon surfaces based on measurements and multidimensional modeling", *Energy Procedi*a, **15**, (2012): 78–83
[EAG03]: S. Eager, N. Mason, T. Bruton, J. Sherborne, R. Russell et al. "Environmentally friendly processes in the manufacture of saturn solar cells", *In Proceedings of the 29th IEEE PVSC*, (2003): 62–65
[EBO08]: A. Ebong, D.S. Kim, A. Rohatgi and W. Zhang. "Understanding the mechanism of light induced plating of silver on screen-printed contacts for high sheet resistance emitters with low surface phosphorous concentration", *In Proceedings of the 33rd IEEE PVSC*, (2008): 1-5.
[EBO10]: A.Ebong, B. Rounsaville, B. Cooper, K.Tate, A. Rohatgi, S. Glunz, M. Horteis. "High efficiency silicon solar cells with ink jetted seed and plated grid on high sheet resistance emitter", *In Proceedings of the 35th IEEE PVSC*, (2010): 1363–1367.
[EBO12]: A. Ebong, "Metallization of crystalline silicon solar cells: a review", *In Proceedings of the 9th International Conference on High Capacity Optical Networks and Enabling Technologies* (HONET), (2012).
[EDW13]: M. Edwards, J. Ji, N. Nampali, et al. "High efficiency with almost no metallization: multiple wire interconnections of plated solar cells", *In Proceedings of the 28th EUPVSEC*, Paris, France, (2013).
[EIN97]: R. Einhaus, E. Vazsony, J. Szlufcik, J. Nijs, and R. Mertens, "Isotropic texturing of multicrystalline silicon wafers with acidic texturing solutions," *In Proceedings of the 26th IEEE PVSC*, (1997): 167-170.
[ENG07]: P. Engelhart, S. Hermann, T. Neubert, et al. "Laser ablation of SiO2 for locally contacted Si solar cells with ultra-short pulses." *Progress in Photovoltaics: Research and Applications* **15**, no. 6 (2007): 521-527.
[ENG13]: J. Engelhardt, S. Ohl, G. Hahn, B. Terheid, "Correlation of Stress in Silicon Nitride Layers with their Complete Removal by Laser Ablation", *Energy Procedia*, **38**, (2013): 707-712
[FAL11]: T. Falcon, "Ultra-fine Line Printing for Silicon Solar Cells: Mesh Screens or Metal Stencils*?"*, *In Proceedings of the 3rd Metallization workshop*, Konstanz, Germany (2011).
[FEL13]: F. Feldmann, M. Bivour, C. Reichel, et al. "A passivated rear contact for high efficiency n-type silicon solar cells enabling high Voc and FF>82%", *In Proceedings of the 28th EUPVSEC*, Paris, France, (2013).
[FEL93]: T.S. Fell, P.R. Wilshaw, M.D. de Coteau, "EBIC investigations of dislocations and their interactions with impurities in silicon", *Physica Status Solidi A Applications and Material Science* **138** (1993) 695.
[FELL11]: T. Fellmeth, A. Born, A. Kimmerle, F. Clement, et al. "Recombination at metal-emitter interfaces of front contact technologies for highly efficient silicon solar cells". *Energy Procedia*, **8**; (2011): 115-121
[FOG04]: J. Foggiato, W. Sik Yoo, M. Ouaknine, T. Murakami, T. Fukada. "Optimizing the formation of nickel silicide", *Materials Science and Engineering B* **114–115** (2004) 56–60
[FRI78]: L. Frisson, P. Lauwers, P. Bulteel, L. De Smet, R. Mertens, R. Govaerts, and R. Van Overstraeten. "Screen printed contacts on silicon solar cells with low series resistance." *In Proceedings of the 13th IEEE PVSC*, (1978): 590-952
[GAB06]: A.M. Gabor, M. Ralli, S. Montminy, L. Alegria, et al. "Soldering induced damage to thin Si solar cells and detection of cracked cells in modules." *In Proceedings of the 21st EUPVSEC*, (2006):2042-2047
[GAL10]: M. Galiazzo, V. Furin, D. Tonini, G. Cellere and A. Baccini, "Double printing of front contacts Ag in c-Si solar cells", *In Proceedings of the 25th EUPVSEC*, (2010): 2338-2340
[GAL13]: S. Gall, J. Vibert, M. Pirot, J-F. Lerat, et al. "Comparison of two picosecond laser sources for SiNx ablation with subsequent nickel silicide formation by excimer laser annealing (ELA) for industrial high efficiency silicon solar cells." *In International Society for Optics and Photonics*, (2013): 882609-882609
[GAL86]: G. Gallagher G, P. Alexander, D. Burger "Flat-plate solar array project final report - Volume V: process development". DOE/JPL-1012-125, Jet Propulsion Laboratory, Pasadena, California. (1986)
[GAM98]: J.P. Gambino and E.G. Colgan , "Silicides and ohmic contacts", *Materials Chemistry and Physics* **52** (1998): 99-146

[GIA11]: A. Giannattasio, A. Giaquinta, and M. Porrin. "The accuracy of the standard resistivity–concentration conversion practice estimated by measuring the segregation coefficient of boron and phosphorous in Cz-Si", *Physica Status Solidi A*, **208**, no. 3; (2011): 564–567
[GLU05]: S.W. Glunz, S. Sterk, R. Steenman, W. Warta, J. Knobloch, W. Wettling, *In Proceedings of the 13th EUPVSEC*, (1995): 409
[GLU07]: S.W. Glunz, "High-Efficiency Crystalline Silicon Solar Cells", *Advances in OptoElectronics*, (2007).
[GOO13]: A. Goodrich, P. Hacke, Q. Wang, B. Sopori, R. Margolis, et al. "A wafer-based monocrystalline silicon Photovoltaics roadmap: Utilizing known technology improvement opportunities for further reductions in manufacturing costs". *Solar Energy Materials and Solar Cells*, **114**; (2013):110–135
[GRA09]: F. Granek. "High efficiency back-contact back-junction silicon solar cells", PhD Thesis, Freiburg, 2009
[GRE81b]: L.A. Grenon, N. G. Sakiotis, and M. G. Coleman. "Reliability of silicon solar cells with a plated nickel-copper metallization system.", *In Proceedings of the 15th PVSC*, (1981): 522-526
[GRE81]: M.A. Green. "Solar cell fill factors: General graph and empirical expressions." *Solid-State Electronics*; **24**, (1981): 788 - 789.
[GRE84]: M. A. Green and S. R. Wenham, Australian Patent No 5703309 Australia, (1984).
[GRE86]: M.A. Green, "Solar cells: operating principles, technology and system applications", UNSW, Kensington (1986).
[GUO05]: J.H. Guo and J.E. Cotter. "Metallization improvement on fabrication of interdigitated backside and double sided buried contact solar cells", *Solar Energy Materials and Solar Cells*, **86**; (2005): 485–498
[HAH10]: G. Hahn, "Status of the selective emitter technology," *In Proceedings of the 25th EUPVSEC*, (2010): 1091-1096
[HAI09]: S.Haiping and X. Qiuxia "Two-step Ni silicide process and influence of protective N2 gas", *Journal of Semiconductors*, **30**, no. 9, (2009): 096002-1 096002-3
[HAL52]: R. N. Hall, "Electron-hole recombination in germanium", *Physical Review*,**87**, (1952): 387
[HAM11]: Z. Hameiri, L. Mai and S. R. Wenham, "Advantages of photoplating for laser doped solar cells", *Progress in Photovoltaics Research and Applications*, **19**; (2011): 511–516
[HAN13]: H. Hannebauer, T. Dullweber, T. Falcon, X. Chen, R. Brendel, "Record low Ag paste consumption of 67.7 mg with dual print", *In Proceedings of the 4th metallization workshop*, Konstanz, Germany, (2013).
[HAR12]: G. Harley, "Progress in mass produced IBC: current status and future opportunities", In Proceedings of the 4th MWT Workshop, (2012)
[HAU11]: J. Haunschild, I.E.Reis, J.Geilker, S.Rein, "Detecting efficiency-limiting defects in Czochralski-grown silicon wafers in solar cell production using photoluminescence imaging", *Physica Status Solidi Rapid Research Letters* **5** (2011)199.
[HAV08]: H. Haverkamp, A. Dastgheib-Shirazi, B. Raabe, F. Book, and G. Hahn. "Minimizing the electrical losses on the front side: development of a selective emitter process from a single diffusion." *In Proceedings of the 33rd IEEE PVSC*, (2008): 1-4
[HEB11]: J. Hebb Y. Wang, S. Shetty, J. McWhirter, D. Owen, M. Shen, V. Le et al. "Laser spike annealing for nickel silicide formation." *In Proceedings of the 22nd Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, (2011): 1-6
[HEI11]: G. Heinrich, M. Bähr, K. Stolberg, T. Wütherich, M. Leonhardt, and A. Lawerenz. "Investigation of ablation mechanisms for selective laser ablation of silicon nitride layers." *Energy Procedia* **8** (2011): 592-597.
[HEI13]: G. Heinrich, A. Lawerenz, "Non-linear absorption of femtosecond laser pulses in a SiNx layer—influence of silicon doping type", *Solar Energy Materials and Solar Cells*, (2013)
[HEN13]: J.B. Heng, J. Fu, B. Kong, Y. Chae, et al. "Commercialization of Tunnel Oxide Junction Based Cell and Module with Efficiency and Good Reliability", *In Proceedings of the 28th EUPVSEC*, Paris, France (2013).
[HER03]: M. Hernandez, J. Venturini, et al. "Laser thermal processing for ultra-shallow junction formation: numerical simulation and comparison with experiments." *Applied Surface Science* **208** (2003): 345-351.
[HER10a]: S. Hermann, NP Harder, R. Brendel, D. Herzog, and H. Haferkamp. "Picosecond laser ablation of SiO2 layers on silicon substrates." *Applied Physics A*, **99**, no. 1 (2010): 151-158
[HER10b]: S. Hermann, T. Dezhdar, NP. Harder, R. Brendel, M. Seibt, and S. Stroj. "Impact of surface topography and laser pulse duration for laser ablation of solar cell front side passivating SiNx layers." *Journal of Applied Physics* **108**, no. 11 (2010): 114514-114514.
[HER11]: A. Herguth, G. Schubert, G. Hahn, I. Melnyk, and M. Käs. "Device for fabricating a photovoltaic element with stabilized efficiency" U.S. Patent Application 12/971,232, filed December 17, 2010.
[HER12]: J.L. Hernández, D. Adachi, K. Yoshikawa, D. Schroos, E. Van Assche, et al. "High efficiency copper electroplated heterojunction solar cells", *In Proceedings of the 27th EUPVSEC*, (2012): 655-656
[HOE06]: B. Hoex, S. B. S. Heil, Erik Langereis, M. C. M. Van de Sanden, and W. M. M. Kessels. "Ultralow surface recombination of c-Si substrates passivated by plasma-assisted atomic layer deposited AlO." *Applied Physics Letters* **89** (2006): 042112.
[HOE12]: M. Van der Hoeven, "World Energy Outlook 2012, Presentation to the press London, 12 November 2012", International Energy Agency, http://www.worldenergyoutlook.org/, retrieved 22 October 2013

[HOL12] Z.C. Holman, A. Descoeudres, L. Barraud, F. Zicarelli Fernandez, J. P. Seif, S. De Wolf, C. Ballif, "Current losses at the front of silicon heterojunction solar cells", *IEEE Journal of Photovoltaics* (2012): 7-15
[HOL13a]: Z.C. Holman, M. Filipic, A. Descoeudres, S. De Wolf, F. Smole, and C. Ballif. "Infrared light management in high-efficiency silicon heterojunction and rear-passivated solar cells." *Journal of Applied Physics* **113**, no. 1 (2013): 013107-013107.
[HOL13b]: Z.C. Holman, A. Descoeudres, S. De Wolf, and C. Ballif. "Record Infrared Internal Quantum Efficiency in Silicon Heterojunction Solar Cells With Dielectric/Metal Rear Reflectors.", *IEEE Journal of Photovoltaics* (2013): 1243 – 1249
[HON08]: K.K.B. Hon , L. Li , I.M. Hutchings, "Direct writing technology—Advances and developments", *CIRP Annals - Manufacturing Technology*, **57**; (2008):601–620
[HOO09]: J. Hoornstra and B. Heurtault, "Stentil print applications and progress for crystalline silicon solar cells", *In Proceedings of the 24th EUPVSEC*, (2009): 989-992
[HOO98]: J Hoornstra, S Roberts, HHC de Moor, et al., "First Experiences With Double Layer Stencil Printing For Low Cost Production Solar Cells", *In Proceedings of the 2nd World PVSEC*, (1998): 1527-1530
[HOR09a]: M.Horteis, "Fine-Line Printed Contacts on Crystalline Silicon Solar Cells", PhD thesis, Freiburg (2008).
[HOR09b]: J. Horzel, "Novel advantageous procedure for inline diffusion of industrial solar cells on mc-Si and EFG-Si material", *In Proceedings of the 24th European PVSEC*, (2009): 1077–1081
[HOR10a]: M. Hörteis, S. W. Glunz "Fundamental Reactions During the Formation of Fired Silver Contacts and Solar Cell Results", *In Proceedings of the 2nd workshop on Metallization for Crystalline Silicon Solar Cells*, Konstanz, Germany (2010).
[HOR10b]: J. Horzel, B. Schum, et al. "On anomalous emitter regions forming during phosphorous diffusion processing of crystalline silicon solar cells", *In Proceedings of the 25th EUPVSEC*, (2010): 1882-1891
[HOR12]: J. Horzel, L. Tous , A. Uruena de Castro, A. Seidl, R. Russell, E. Cornagliotti. "CZ-Si material influence on PERL-type Si solar cells". *In Proceedings of the 27th EUPVSEC*, (2012): 780-788
[HSU09]: H.F. Hsu, C. L. Tsai, et al. "Mechanism of immersion deposition of Ni–P films on Si (100) in an aqueous alkaline solution containing sodium hypophosphite." *Thin Solid Films 517*, no. 17 (2009): 4786-4791.
[HUE09]: K. Huet, G. Fisicaro, J. Venturini, H. Besaucèle, et al. "Defect kinetics and dopant activation in submicrosecond laser thermal processes." *Applied Physics Letters* **95**, no. 23 (2009): 231901-231901.
[HUE12]: K. Huet, "Ultra-Low Thermal Budget Laser Thermal Annealing for 3D Semiconductor and Photovoltaic Applications." (2012).
[HUS05]: F. Huster, "Investigation of the alloying process of screen printed aluminum pastes for the BSF formation on silicon solar cells", *In Proceedings of the 20th EUPVSEC*, (2005).
[IMB08]: B. Imbert , S. Zoll , P. Garnier, B. Pernet, D. Galpin, R. Beneyton, M. Juhel, et al. "Self-aligned nickel–platinum silicide oxidation", *Materials Science and Engineering B* **154–155** (2008) 155–158
[IPC13]: IPCC fifth Assessment Report, "Climate Change 2013: The Physical Science Basis, IPCC WGI AR5", http://www.climatechange2013.org/, retrieved 22 October 2013
[IST98]: A.A. Istratov and E.R.Weber. "Electrical properties and recombination activity of copper, nickel and cobalt in silicon", *Applied Physics A*, **66**; 6 (1998): 123-136
[ITR13]: International Technology Roadmap for Photovoltaic (ITRPV) Edition 2013 , http://www.itrpv.net/, retrieved on 22 October 2013
[IWA02]: H. Iwai, T. Ohguro, and S. Ohmi. "NiSi salicide technology for scaled CMOS", *Microelectronic Engineering*, **60** (2002): 157-169
[JAG86]: Jager, K., and R. Hezel. "Optical stability of silicon nitride MIS inversion layer solar cells." *IEEE Transactions on Electron Devices* **32**, no. 9 (1985): 1824-1829.
[JEN03]: J.A.D. Jensen, P. Møller, T. Bruton, et al., "Electrochemical Deposition of Buried Contacts in High-Efficiency Crystalline Silicon Photovoltaic Cells", *Journal of The Electrochemical Society*, **150**; (2003): 49-57
[JON05]: P.C. de Jong, D. W. K. Eikelboom, J. A. Wienke, M. W. Brieko, and M. J. H. Kloos. "Low-Stress Interconnections for Solar Cells." *In Proceedings at the 20th EUPVSEC*, (2005): 10-14
[KAL13]: A. Kalio, A. Richter, M. Glatthaara, J. Wilde, "Study of Contact Formation of Printed Contacts Through Different Passivation Layers on Lowly Doped Emitters", *Energy Procedia* **38** (2013): 745-752.
[KAM11]: M. Kamp, J. Bartsch, S. Nold, M. Retzlaff, M. Hörteis, S. W. Glunz. "Economic Evaluation of Two-Step Metallization Processes for Silicon Solar Cells", *Energy Procedia* **8** (2011): 558-564.
[KAN04]: N. Kanani, "Electroplating: basic principles, processes and practice", Elsevier, (2004): 353
[KAR10]: A. Karpour, "Advanced Electroless Metallisation of High Efficiency Laser Doped and Inkjet Printed Silicon Solar Cells." *Master thesis*, UNSW, Sydney (2010).
[KER02]: M. Kerr, "Surface, emitter and bulk recombination in silicon and development of silicon nitride passivated solar cells", *PhD Thesis*, The Australian national University (ANU), Australia, (2002).
[KIM11]: S-K. Kim, H-S. Ee, W. Choi, S-H. Kwon, J-H. Kang, Y-H. Kim, et al. "Surface-plasmon-induced light absorption on a rough silver surface." *Applied Physics Letters*, **98**, no. 1 (2011): 011109-011109.
[KIM12]: A. Kimmerle, M. Rüdiger, A. Wolf, M. Hermle, D. Biro, "Validation of analytical modeling of locally contacted solar cells by numerical simulations." *Energy Procedia*, **27**, 219-226 (2012).

[KIN91]: D. L. King and M. E. Buck, “Experimental optimization of an anisotropic etching process forrandom texturization of silicon solar cells,” *In Proceedings of the 22nd IEEE PVSC*, (1991): 303-308
[KIT07]: J. A. Kittl, M. A. Pawlak, C. Torregiani, A. Lauwers, C. Demeurisse, C. Vrancken, P. P. Absil, and S. Biesemans. "Transient and end silicide phase formation in thin film Ni/polycrystalline-Si reactions for fully silicided gate applications." *Applied Physics Letters,* **91** (2007): 172108.
[KIT08]: J.A. Kittl, K. Opsomer, C. Torregiani, C. Demeurisse, S. Mertens, et al. "Silicides and germanides for nano-CMOS applications." *Materials Science and Engineering B* **154** (2008): 144-154.
[KNO09a]: A. Knorz, M. Aleman, A. Grohe, R. Preu, et al. "Laser ablation of antireflection coatings for plated contacts yielding solar cell efficiencies above 20%." *In Proceedings of the 24th EUPVSEC*, (2009): 1002-1005
[KNO09b]: A. Knorz, M. Peters, A. Grohe, C. Harmel, and R. Preu. "Selective laser ablation of SiNx layers on textured surfaces for low temperature front side metallizations." *Progress in Photovoltaics: Research and Applications* **17**, no. 2 (2009): 127-136.
[KOB13] E. Kobayashi, N. Nakamura, K. Hashimoto, Y. Watabe. "Rear-Emitter Silicon Heterojunction Solar Cells with Efficiencies above 22%", *In Proceedings of the 28th EUPVSEC*, (2013).
[KOH09]: A. Kohn and M. Eizenberg. "Diffusion barriers for ultra-large-scale integrated copper metallization." *Nanoscale ULSI Interconnects: Fundamentals and Applications*, (2009): 93-120
[KOS13]: E. Kossen, I. Romijn, K. Tool, "Cost reduction n-Pasha by improved metallization", *In Proceedings of the 4th metallization workshop*, Konstanz, Germany, (2013).
[KRA08]: D. Kray, M. Alemán, A. Fell, S. Hopman, K. Mayer, et al. "Laser-doped Silicon Solar Cells by Laser Chemical Processing (LCP) exceeding 20% Efficiency", *In Proceedings of the 33rd IEEE PVSC*, (2008): 1-3
[KUD08]: S. Kudo, Y. Hirose, N. Hashikawa, T. Yamaguchi, et al. "Analysis of Ni silicide abnormal growth mechanism using advanced TEM techniques." *In IEEE Reliability Physics Symposium*, (2008): 580-583
[KUL12]: P.K. Kulshreshtha, Y. Yoon, K.M. Youssef, E.A. Good, G. Rozgonyi, "Oxygen precipitation related stress-modified crack propagation in high growth rate Czochralski silicon wafers", *Journal of the Electrochemical Society*, **159**, (2012) H125.
[KUR11]: S. Kurtz, K. Whitfield, G. TamizhMani, M. Koehl, et al. "Evaluation of high-temperature exposure of photovoltaic modules." *Progress in Photovoltaics: Research and applications* **19**, no. 8 (2011): 954-965.
[KVE01]: V. Kveder, M. Kittler, W. Schröter, "Recombination activity of contaminated dislocations in silicon: a model describing electron-beam-induced current contrast behavior", *Physical Review B: Condensed Matter* **63** (2001) 115208.
[KYE12]: D. Kyeong, S.-H. Cho, et al. "Approaching 20%-Efficient Selective-Emitter Solar Cells with Copper Front Contacts on Industrial 156 mm Cz Si Wafers", *In Proceedings of the 27th EUPVSEC*, (2012): 600-303
[LAC12]: A. Lachowicz, K. Ramspeck, E. Brouwer, B. Schum, A. Metz et al. "Nox-Free Solution for Emitter Etch-Back", *In Proceedings of the 27th EUPVSEC*, (2012): 1846-1850
[LAU01]: A Lauwers, A. Steegen, M. de Potter, R. Lindsay, A. Satta, et al. "Materials aspects, electrical performance, and scalability of Ni silicide", Jour*nal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **19**, no. 6 (2001): 2026-2037.
[LAU04]: A. Lauwers, JA. Kittl, M. J.H. Van Dal, O. Chamirian, MA. Pawlak, M. de Potter, et al. "Ni based silicides for 45 nm CMOS and beyond" *Materials Science and Engineering B* **114–115** (2004): 29–41
[LAU11a]: G. Laudisio et al., “Reduced contact resistance of new FS silver pastes towards fine line printing and cost reduction”, *In Proceedings of the 3rd Metallization workshop*, Konstanz, Germany (2011).
[LAU11b]: T. Lauermann, A. Zuschlag, S. Scholz, et al. "The influence of contact geometry and sub-contact passivation on the performance of screen-printed Al2O3 passivated solar cells." *In Proceedings of the 26th EUPVSEC*, (2011): 1137-1143.
[LAV03]: C. Lavoie, F.M. d’Heurle, C. Detavernier, and C. Cabral Jr. “Towards implementation of a nickel silicide process for CMOS technologies.”, *Microelectronic Engineering*, **70**; (2003): 144–157.
[LEE00]: P.S. Lee, D. Mangelinck, K.L. Pey, J. Ding, J.Y. Dai, C.S. Ho, A. See "On the Ni–Si phase transformation with and without native oxide", *Microelectronic Engineering* **51–52** (2000): 583–594
[LEE06]: R.T.P. Lee, T-Y. Liow, et al. "Novel nickel-alloy silicides for source/drain contact resistance reduction in N-channel multiple-gate transistors with sub-35nm gate length." *In Electron Devices Meeting*, (2006): 1-4
[LEE11]: E. Lee, H. Lee, J. Choi, D. Oh, J. Shim, et al. "Improved LDSE processing for the avoidance of overplating yielding 19.2% efficiency on commercial grade crystalline Si solar cell." *Solar Energy Materials and Solar Cells* **95**, no. 12 (2011): 3592-3595.
[LEN12]: A. Lennon, Y. Yao and S.R. Wenham, "Evolution of metal plating for silicon solar cell metallization", *Progress in Photovoltaics Research and Applications*, **21**(7); (2013)1454-1468
[LI11]: T. Li, C. Lan Zhou, Z. Gang Liu, et al. "Improved Ghost Plating of Light-Induced Plating on Crystalline Silicon Solar Cells by SiO2/SiN Selective Etching." *Applied Mechanics and Materials* **71** (2011): 2290-2293.
[LI13]: H. Li, SR Wenham, and Z. Shi. "High efficiency PERL cells on CZ P-type crystalline silicon using a thermally stable a-Si:H/SiNx rear surface passivation stack." *Solar Energy Materials and Solar Cells* **117** (2013): 41-47.

[LIM10]: L. Bianca, K. Bothe, and J. Schmidt. "Impact of oxygen on the permanent deactivation of boron–oxygen-related recombination centers in crystalline silicon." *Journal of Applied Physics* **107**, no. 12 (2010): 123707-123707.
[LIM11]: L. Bianca, V.V. Voronkov, R. Falster, K. Bothe, and J. Schmidt. "Lifetime recovery in p-type Czochralski silicon due to the reconfiguration of boron–oxygen complexes via a hole-emitting process." *Applied Physics Letters* **98**, no. 16 (2011): 162104-162104.
[LIU05]: C.M. Liu, W.L. Liu, W.J. Chen, S.H. Hsieh, T.K. Tsai, and L.C. Yang. "ITO as a diffusion barrier between Si and Cu." *Journal of The Electrochemical Society* **152**, no. 3 (2005): G234-G239.
[MAC04]: D. Macdonald, and L. J. Geerligs. "Recombination activity of interstitial iron and other transition metal point defects in p-and n-type crystalline silicon", *Applied Physics Letters* **85**, no. 18 (2004): 4061-4063.
[MAC07]: D. Macdonald, and J. Tan. "Impurities in solar-grade silicon." *In Microelectronics, MEMS, and Nanotechnology, International Society for Optics and Photonics*, (2007): pp. 68000X-68000X
[MAL90]: G. Mallory and J. Hajdu, "Electroless plating: fundamentals and applications", Orlando, USA, (1990).
[MAN62]: J. Mandelkorn, C. McAfee, J. Kesperis, L. Schwartz, and W. Pharo, "Fabrication and characteristics of phosphorous-diffused silicon solar cells", *Journal of the Electrochemical Society*, **109**(4); (1962): 313–318
[MAN73]: J. Mandelkorn, and John H. Lamneck. "A new electric field effect in silicon solar cells." *Journal of Applied Physics* **44**, no. 10 (1973): 4785-4787.
[MAS06]: N. Mason, O. Schultz, R. Russell, S. Glunz, and W. Warta. "20.1% efficient large area cell on 140 micron thin silicon wafer", *In Proceedings of the 21st EUPVSEC*, (2006)
[MAY70]: A.F. Mayadas, M. Shatzkes, "Electrical-Resistivity Model for Polycrystalline Films: the Case of Arbitrary Reflection at External Surfaces", *Physical Review B*, **1**, no 4, (1970):1382-1389
[MCI01]: K.R. McIntosh, "Lumps Humps and Bumps: Three Detrimental Effects in the Current Voltage Curve of Silicon Solar Cells", *PhD thesis*, Sydney (2001).
[MCI12]: K. R. McIntosh and S. C. Baker-Finch, "OPAL 2: Rapid optical simulation of silicon solar cells," *In Proceedings of the 38th IEEE PVSC*, (2012): 265–271.
[MER12]: V.Mertens, T. Ballmann, J.Y. Lee, M. Junghänel, et al. "Industrial High Influence of base resistivity on solar cell parameters of double-side contacted rear junction solar cells". *Energy Procedia*, **27**; (2012): 53-58
[MER13]: V. Mertens, T. Ballmann, J. Cieslak, et al. "Large Area n-Type Cz Double Side Contact Back Junction Solar Cell with 21.3% Conversion Efficiency". *In Proceedings of the 28th EUPVSEC*, Paris, (2013).
[MET07]: A. Mette, "New concepts for front side metallization of industrial Si solar cells", *PhD thesis*, Freiburg (2007).
[MET12]: A. Mette, F. Stenzel, A. Hofmann, St. Hörnlein, T. Florian et al., "Evaluation of fine line printing and plating in pilot production at Q-Cells", *In Proceedings of the 3rd workshop on Metallization for Crystalline Silicon Solar Cells*, Charleroi, Belgium (2012).
[MET13]: A. Metz, D. Adler, S. Bagus, H. Blanke, M. Bothar, E. Brouwer, S. Dauwe et al. "Industrial high performance crystalline silicon solar cells and modules based on rear surface passivation technology." *Solar Energy Materials and Solar Cells* (2013).
[MON13]: A. Mondon, M. N. Jawaid, J. Bartsch, M. Glatthaar, and S. W. Glunz. "Microstructure analysis of the interface situation and adhesion of thermally formed nickel silicide for plated nickel–copper contacts on silicon solar cells." *Solar Energy Materials and Solar Cells* **117** (2013): 209-213.
[MOS12]: F. Mosel, A. Molchanov, B. Fischer, et al., "Growth of High Quality Silicon Mono Ingots by the Application of a Magnetic Cusp Field in Cz-Puller", *In Proceedings of the 27th EUPVSEC*, (2012): 933 – 938
[MUL08]: W.P.Mulligan, T. Pass, D. Smith, N. Kaminar, K.R. McIntosh, R.M. Swanson. "Solar cell and method of manufacture", US 7,229,110, (2008).
[MUL12]: J. Müller, K. Bothe, S. Gatz, and R. Brendel. "Modeling the formation of local highly aluminum doped silicon regions by rapid thermal annealing of screen printed aluminum." *Physica Status Solidi Rapid Research Letters* **6**, no. 3 (2012): 111-113.
[MUN12]: D. Muñoz, T. Desrues, A.-S. Ozanne, et al., "Key aspects on development of high efficiency heterojunction and IBC heterojunction solar cells: towards 22% efficiency on industrial size", *In Proceedings of the 27th EUPVSEC*, (2012): 577-579
[MUR13]: J.D. Murphy, R.E. McGuire, K. Bothe, V.V. Voronkov, R.J. Falster, "Minority carrier lifetime in silicon Photovoltaics: The effect of oxygen precipitation", *Solar Energy Materials and Solar Cells* (2013), http://dx.doi.org/10.1016/j.solmat.2013.06.018
[MUR95]: S.P. Murarka, "Review: silicide thin films and their application in microelectronics", *Intermetallics* **3** (1995):173-186.
[MUS13]: C. Muschelknautz, A. Henning, et al., "Standard Printing Techniques – Pushing the Envelope to 75 mg Paste per Cell", *In Proceedings of the 4th metallization workshop*, Konstanz, Germany, (2013).
[NEU07]: D-H Neuhaus and A. Munzer, "Industrial Silicon Wafer Solar Cells", *Advances in OptoElectronics*, (2007).
[NGA12]: M. Ngamo, L. Tous, E. Cornagliotti, J. Horzel, et al. "Integration of high sheet resistance homogeneous emitters in a process flow for PERC-type solar cells with Cu contacts." *In Proceedings of the 38th IEEE PVSC*, (2012):3371-3376.

[NIC81]: M-A. Nicolet and M. Bartur. "Diffusion barriers in layered contact structures." *Journal of Vacuum Science and Technology* **19**, no. 3 (1981): 786-793.
[PAL07]: D. W. Palmer, K. Bothe and J. Schmidt, "Kinetics of the electronically stimulated formation of a boron-oxygen complex in crystalline silicon", *Physical Review B* **76**, (2007).
[PAL85]: E.D. Palik, "Handbook of Optical Constants of Solids Vol I", Academic Press, (1985): 577–580
[PAP13]: P. Papet, T. Söderström, et al., "Front grid metallization and module interconnections of industrial heterojunction solar cells", *In Proceedings of the 4th metallization workshop*, Konstanz, Germany (2013).
[PRA12]: V. Prajapati, J. Horzel, P. Choulat, T. Janssens, J. Poortmans, R. Mertens, "Oxidation enhanced diffusion for screen printed silicon solar cells", *In Proceedings of the 38th IEEE PVSC*, (2012): 1089-1093
[PRA13]: V. Prajapati, "Advanced front side technology in crystalline silicon solar cells", *PhD thesis*, KULeuven, (2013).
[PRE00]: R. Preu, S.W. Glunz, et al. "Laser ablation-A new low-cost approach for passivated rear contact formation in crystalline silicon solar cell technology." *In Proceedings of the 16th EUPVSEC*, (2000): 1181-1184
[PSY09]: D. Pysch, A. Mette, A. Filipovic and S. W. Glunz, "Comprehensive Analysis of Advanced Solar Cell Contacts Consisting of Printed Fine-line Seed Layers Thickened by Silver Plating", *Progress in Photovoltaics Research and Applications*, **17**; (2009): 101–114.
[PVI13]: Average 156 mm Mono Solar Cell and Wafer Weekly Spot Prices, http://pvinsights.com/, retrieved on 22 October 2013.
[PYS07]: D. Pysch, A. Mette, A. Filipovic, and S. W. Glunz "Detailed analysis of fine line printed and planted solar cell contacts", *in Proceedings of the 22nd EUPVSEC*, (2007).
[RAL75]: E.L. Ralph, "Recent advancements in low cost solar cell processing." *In Proceedings of the 11th IEEE PVSC*, (1975): 315
[RAN91]: J.A. Rand and P.A. Basore, "Light Trapping Silicon Solar Cells Experimental Results and Analysis", *In Proceedings of the 22nd IEEE PVSC*, (1991): 192-197
[RAP12]: K. Rapolu, K. Wijekoon, P. Kumar, F. Yan, A. Chan, L. Zhang, et al. "Performance Comparison of High Efficiency Parasitic Rear Emitter Etched Solar Cells with Conventional Silicon Solar Cells", *In Proceedings of the 27th EUPVSEC*, (2012): 1912-1916
[RAU11]: M. Rauer, C. Schmiga, R. Woehl, K. Ruhle, M. Hermle, et al. "Investigation of aluminum-alloyed local contacts for rear surface-passivated silicon solar cells." *IEEE Journal of Photovoltaics*, **1** (2011): 22-28.
[RAU13]: M. Rauer, C. Schmiga, M. Glatthaar, and S.W. Glunz, "Alloying From Screen-Printed Aluminum Pastes Containing Boron Additives", *IEEE Journal of Photovoltaics*, **3**(1); (2013): 206-211
[RAU13b] M. Rauer, A. Mondon, C. Schmiga, J. Bartsch, M. Glatthaar, and S. W. Glunz. "Nickel-plated front contacts for front and rear emitter silicon solar cells." *Energy Procedia* **38** (2013): 449-458.
[REC13]: M Recamán Payo, N. Posthuma, A. Urueña de Castro, et al. "Boron-doped selective silicon epitaxy: high efficiency and process simplification in interdigitated back contact cells", *Progress in Photovoltaics Research and Applications*, DOI: 10.1002/pip.2427
[REI07]: K.A. Reinhardt, Kern W, "Handbook of Silicon Wafer Cleaning Technology", William Andrew, Norwich, NY, USA, (2007).
[RIC04]: B. S. Richards, "Comparison of TiO2 and Other Dielectric Coatings for Buried contact Solar Cells: a Review", *Progress in Photovoltaics Research and Applications*, **12**; (2004): 253–281
[RIC12]: A. Richter, F. Werner, A. Cuevas, J. Schmidt, SW Glunz, "Improved parameterization of auger recombination in silicon" *Energy Procedia*, **27**, (2012): 88–94
[RIC13]: D. Richards, Plating for high efficiencies, Photon International 2013 July: 118-125
[RIC97]: G. Richardson, and B. Stein. "Comparative study of three internal stress measurement methods." In AESF Electroforming Symposium, San Diego, CA, USA. (1997).
[RIE91]: W. Riedel, "Electroless Nickel Plating", Finishing Publications LTD./ASM international, Stevengae, England, OH, USA, (1991).
[RIV05]: C. Rivero, P. Gergaud, M. Gailhanou, O. Thomas, B. Froment, H. Jaouen, and V. Carron. "Combined synchrotron x-ray diffraction and wafer curvature measurements during Ni–Si reactive film formation." *Applied Physics Letters* **87**; 4 (2005): 041904.
[ROD10]: T. C. Röder, E. Hoffmann, J. R. Köhler, and J. H. Werner. "30 μm wide contacts on silicon cells by laser transfer", *In Proceedings of the 35th IEEE PVSC*, (2010).
[ROH10]: A. Rohatgi, D. Meier, et al. "Developing novel low-cost, high-throughput processing techniques for 20%-efficient monocrystalline silicon solar cells", *in Photovoltaics International*, **10** (2010) 87-94.
[ROU13]: A. Rouhi, "Investigation on light induced plating of nickel for novel front contact schemes of silicon solar cells", *Master thesis*, KULeuven, (2013).
[RUD13]: D. Rudolph, S. Olibet, J. Hoornstra, A. Weeber, E. Cabrera, A. Carr, M. Koppes, R. Kopecek, "Replacement of silver in silicon solar cell metallization pastes: Is it possible?", *In Proceedings of the 4th metallization workshop*, Konstanz Germany, (2013).
[RUS12]: R. Russell, L. Tous, H. Philipsen, J. Horzel, et al. "A Simple Copper Metallization Process for High Cell Efficiencies and Reliable Modules", *In Proceedings of the 27th EUPVSEC*, (2012): 538-543

[SAN09]: MC. Sanchez and N. Stem. "Phosphorus emitter and metal - grid optimization for homogeneous (n+p) and double-diffused (n++n+p) emitter silicon solar cells", *Materials Research*, **12**; (2009): 57-62
[SCH06]: A. Schneider, L. Rubin, and G. Rubin, "Solar cell efficiency improvement by new metallization techniques -the day4TM electrode concepts", *In Proceedings of the 4th WCPSC*, (2006): 1095-1098
[SCH06]: G. Schubert, "Thick Film Metallization of Crystalline Silicon Solar Cells Mechanisms, Models and Applications", *PhD thesis*, Konstanz, (2006).
[SCH08]: J. Schmidt, A. Merkle, Rolf Brendel, Bram Hoex, MCM van de Sanden, and W. M. M. Kessels. "Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al2O3." *Progress in Photovoltaics: research and applications* **16**, no. 6 (2008): 461-466.
[SCH09]: P. Schmuki, and S. Virtanen, "Electrochemistry at the Nanoscale". Springer, (2009).
[SCH10]: C. Schmiga, M. Rauer, M. Rüdiger, K. Meyer, J. Lossen, et al. "Aluminium-doped p+ silicon for rear emitters and back surface fields: Results and potentials of industrial n-and p-type solar cells." *In Proceedings of the 25th EUPVSEC*, (2010): 1163-1168.
[SCH13]: J. Schön, A. Abdollahinia, R. Müller, J. Benick, M. Hermle, W. Warta, MC. Schubert "Predictive simulation of doping processes for silicon solar Cells", *Energy Procedia*, **38**, (2013): 312-320
[SCH39]: W. Schottky, "Zur Halbleitertheorie der Sperrschicht- und Spitzengleichrichter", Z. Physik, 113, (1939): 67-414
[SCH52]: W. Shockley and W. T. J. Read, "Statistics of the recombinations of holes and electrons", *Physical Review*, **87**, (1952): 835-842
[SCH64]: W. Shockley, W. W. Hooper, H. J. Queisser, et al. " Mobile Electronic Charges on Insulating Oxides with Application to Oxide Covered Silicon P-N Junctions," *Surface Science*, vol. 2, (1964): 277-287
[SCH78]: D.K. Schroder, R.N. Thomas, J.C. Swartz, "Free carrier absorption in silicon", *IEEE journal of solid state circuits*, **13**, (1978): 180-187
[SCH84]: D.K. Schroder and D. L. Meier, "Solar cell contact resistance - a review", *IEEE Transactions on Electron Devices*, **31**, (1984): 637-647
[SCH90]: D.K. Schroder, "Semiconductor material and device characterization", John Wiley & Sons, (1990).
[SEI90]: H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel. "Anisotropic etching of crystalline silicon in alkaline solutions I. Orientation dependence and behavior of passivation layers." *Journal of the electrochemical society* **137**, no. 11 (1990): 3612-3626.
[SET06]: Y. Setiawan, P. S. Lee, K. L. Pey, X. C. Wang, G. C. Lim, and F. L. Chow. "Laser Annealed Ni (Ti) Silicides Formation." *In Proceedings of the 14th IEEE Conference on Advanced Thermal Processing of Semiconductors*, (2006): 223-227
[SHI13]: A. Dastgheib-Shirazi , M. Steyer , G. Micard , et al. "Relation between Diffusion Parameters and Phosphorus Precipitation during the POCI3-Diffusion Process", *Energy Procedia*, **38**, (2013): 254–262
[SHU06]: O. Schultz, S.W. Glunz, W. Warta, R. Preu, et al. "High-efficiency solar cells with laser-grooved buried contact front and laser-fired rear for industrial production." *In Proceedings of the 21st EUPVSEC*, (2006).
[SIN00]: R.A. Sinton, and A. Cuevas, "A Quasi-Steady-State Open-Circuit Voltage Method for Solar Cell Characterization," In Proceedings of the 16th EUPVSEC, (2000).
[SON13]: R. Søndena,Y.Hu, M. Juel, M.S.Wiig, et al., "Characterization of the OSF- band structure in n-type Cz-Si using photoluminescence-imaging and visual inspection", *Journal of Crystal Growth*, **367**, (2013):68.
[STA05]: M. Stangl, J. Acker, V. Dittel, et al. "Characterization of electroplated copper self-annealing with investigations focused on incorporated impurities." *Microelectronic engineering*, **82**(2), (2005): 189-195.
[STA09]: N. Stavitski, "Silicide-to-silicon specific contact resistance characterization, test structures, and models", *PhD thesis*, Leuven (2009).
[STE13]: B. Steinhauser, MB Mansoor, et al. "Passdop based on firing stable a-SiNx:P as a concept for the industrial implementation of n-type PERL silicon solar cells", *In Proceedings of the 28th EUPVSEC*, (2013).
[SUG11]: A. Sugianto, "Development of Commercial, High-efficiency Silicon Solar Cells Incorporating Selective Emitters and Passivated Rear Contacts", *PhD thesis*, UNSW (2011).
[SUL57]: M. V. Sullivan and J. H. Eigler, "Electroless nickel plating for making ohmic contacts", *Journal of the Electrochemical Society*, **104**, (1957): 226-230
[SWA05]: R. M. Swanson, "Approaching the 29% limit efficiency of silicon solar cells", *In Proceedings of the 31st IEEE Photovoltaic Specialists Conference*, (2005).
[SYN12]: Synopsys. (2012). Synopsys TCAD, release G-2012.06. Available: http://www.synopsys.com
[SZL06]: J. Szlufcik, G. Agostinelli, F. Duerinckx, E. Van Kerschaver, G. Beaucarne "Low Cost Industrial Technologies of Crystalline Silicon Solar Cells" Chapter IIb-2 in "Solar Cells: Materials Manufacture and Operation" Edited by Markvart and Castañer, Elsevier, Amsterdam, The Netherlands (2006).
[TAK00]: N. Takano, N. Hosoda, T. Yamada, and T. Osaka. "Mechanism of the chemical deposition of nickel on silicon wafers in aqueous solution." Journal of The Electrochemical Society 146, no. 4 (1999): 1407-1411.
[TAN02]: W. L. Tan and K. L. Pey, Simon Y. M. Chooi, et al. "Effect of a titanium cap in reducing interfacial oxides in the formation of nickel silicide", *Journal of Applied Physics*, **91**, no. 5 (2002): 2901-2909.
[TEO01]: V. Teodorescu, L. Nistor, H. Bender, et al., "In situ transmission electron microscopy study of Ni silicide phases formed on (001) Si active lines", *Journal of applied physics*, **90**, no. 1 (2001): 167-174.

[THE12]: The outlook for silver industrial demand, commissioned by the silver institute, http://www.silverinstitute.org/site/publications/, retrieved on November, 10th, 2012.
[THE13]: "How to lose half a trillion euros", published on October 12th 2013 in The Economist, http://www.economist.com/news/briefing/21587782-europes-electricity-providers-face-existential-threat-how-lose-half-trillion-euros, retrieved on October, 22nd, 2013.
[THI13]: S. Thibert, J. Jourdan, B. Bechevet, D. Chaussy, et al., "Emitter Requirements for Nickel Contacts on Silicon Solar Cells-A Simulation Study." *Energy Procedia* **38** (2013): 321-328.
[TJA08]: B. Tjahjono, S. Wang, A. Sugianto, L. Mai, N. Borojevic, et al. "Application of laser doped contact structure on multicrystalline solar cells." *In Proceedings of the 23rd EUPVSEC*, (2008): 1995-2000
[TJA10]: B.S. Tjahjono, "Laser doped selective emitter solar cells", *PhD thesis*, UNSW (2010).
[TOU13]: L. Tous, J-F. Lerat, T. Emeraud, et al. "Nickel silicide contacts formed by excimer laser annealing for high efficiency solar cells", *Progress in Photovoltaics: Research and Applications*, **21**, no 3, (2013): 267–275
[TSU04]: M. Tsuchiaki, K. Ohuchi, et al. "Junction leakage generation by NiSi thermal instability characterized using damage-free n+/p silicon diodes." *Japanese Journal of Applied Physics*, 43, (2004): 5166–5173
[TUR13]: G. Turner, "Global renewable energy market outlook 2013 fast pack, 22 April 2013", Bloomberg New Energy Finance, http://about.newenergyfinance.com/about/, retrieved 22 October 2013
[URR10]: E. Urrejola, K. Peter, H. Plagwitz, and Gunnar Schubert. "Al-Si alloy formation in narrow p-Si contact areas." *In Proceedings of the 2nd Workshop on Metallization of Crystalline Silicon Solar Cells*. (2010).
[URR12]: E. Urrejola, "Aluminum-silicon formation through dielectric openings: Application to industrial rear passivated high efficiency solar cells", *PhD thesis*, Konstanz University (2012).
[URU12a]: A. Uruena, J. Horzel, J. John, E. Cornagliotti, et al. "Interaction between Al–Si melt and dielectric layers during formation of local Al alloyed contacts for rear passivated Si solar cells." *Physica Status Solidi A*, **209**, no. 12 (2012): 2615-2619.
[URU12b]: A. Uruena, J. Horzel, S. Singh, I. Kuzma-Filipek, E. Cornagliotti, et al. "Rear contact and BSF formation for local Al-BSF solar cells." *Energy Procedia* **27** (2012): 561-566.
[URU13a]: A. Uruena, "Advanced rear-side contact schemes on i-PERC (industrial passivated emitter and rear cell) solar cells", *PhD thesis*, KULeuven, Leuven (2013).
[URU13b]: A. Uruena, L. Tous, F. Duerinckx, I. Kuzma-Filipek, et al., "Understanding the Mechanisms of Rear Reflectance Losses in PERC Type Silicon Solar Cells" *Energy Procedia*, **38**, (2013): 801-806
[VAN09]: C. Van Bockstael, C. Detavernier, R. L. Van Meirhaeghe, J. L. Jordan-Sweet, and C. Lavoie "In situ study of the formation of silicide phases in amorphous Ni–Si mixed layers." *Journal of Applied Physics* **106** (2009): 064515.
[VEN04]: J. Venturini, M. Hernandez, G. Kerrien, C. Laviron, D. Camel, et al. "Excimer laser thermal processing of ultra-shallow junction: laser pulse duration." *Thin solid films* **453** (2004): 145-149.
[VEN12]: J. Venturini, "Laser Thermal Annealing: Enabling ultra-low thermal budget processes for 3D junctions formation and devices." *In Proceedings of the 12th* IWJT, (2012): 57-62
[VER12a]: B. Vermang, "Aluminum oxide as negatively charged surface passivation for industrial crystalline silicon solar cells", *Phd Thesis*, KULeuven (2012).
[VER12b]: B. Vermang, H. Goverde, L. Tous, et al. "Approach for Al2O3 rear surface passivation of industrial p-type Si PERC above 19%". *Progress in Photovoltaics Research and Applications*, **20**; (2012): 269-273
[VER12c] PJ. Verlinden PJ et al. "Simple power-loss analysis method for high-efficiency Interdigitated Back Contact (IBC) silicon solar cells" *Solar Energy Materials and Solar Cells*, **106** (2012): 37–41
[VER13]: P.J. Verlinden, "Cost Analysis of Current Production and Strategy for Future Silicon PV Modules", *In Proceedings of the 28th EUPVSEC*, Paris, France (2013)
[VON12]: H. von Campe, S. Huber, S.Meyer, S. Reif, J. Vietor. "Direct tin-coating of aluminum rear contact by ultrasonic soldering". *In Proceedings of the 27th EUPVSEC*, (2012): 1150-1153
[VOR10]: V.V. Voronkov, R.J. Falster, J. Schmidt, K. Bothe, and A. Batunina. "Lifetime Degradation in Boron Doped Czochralski Silicon." *ECS Transactions* **33**, no. 11 (2010): 103-112.
[WAN09]: S. Wang, T. Puzzer, et al. "Overcoming over-plating problems on acid textured multicrystalline wafers with silicon nitride coated surfaces." *In Proceedings of the 24th EUPVSEC*, (2009): 1449-1452.
[WAN12]: A. Wang, P. Han, H.Lu, H. Qian, L. Chen, et al. "Advanced PERC and PERL production cells with 20.3% record efficiency for standard commercial p-type silicon wafers". *Progress in Photovoltaics Research and Applications*, **20**; (2012): 260–268.
[WAN94]: S.Q. Wang "Barriers Against Copper Diffusion into Silicon and Drift Through Silicon Dioxide" MRS Bulletin, (1994): 30-40
[WEB83]: E.R. Weber, "Transition metals in silicon." *Applied Physics A* **30**, no. 1 (1983): 1-22.
[WEH11]: N. Wehkamp, A. Fell, J. Bartsch, F. Granek. "Laser Chemical Metal Deposition for Silicon Solar Cell Metallization", *In Proceedings of the 3rd metallization workshop*, Charleroi, Belgium, (2011).
[WEI07]: D. Weisser, "A guide to life-cycle greenhouse gas (GHG) emissions from electric supply technologies." *Energy* 32, no. 9, (2006): 1543-1559.
[WEN10]: A.M. Wenham, M.A. Green, and S. R. Wenham. "METAL ADHESION." U.S. Patent Application 13/254,631, filed February 24, 2010.

[WEN12]: J. Wendt, M. Träger, M. Mette, et al. "The link between mechanical stress induced by soldering and micro damages in silicon solar cells." *In Proceedings of 24th EUPVSEC*, (2009): 3420-3423.
[WEN96]: S.R. Wenham, C.B. Honsberg, S. Edmiston, L. Koschier et al. "Simplified buried-contact solar cell process". *In Proceedings of the 25th PVSC*, (1996): 389–392.
[WOL00]: S. Wolf, R. N. Tauber, "Silicon Processing for the VLSI Era: Process Technology", *In Silicon Processing for the VLSI Era Volume 1*, Lattice Press, (2000)
[WOL10]: A. Wolf, D. Biro, J. Nekarda, S. Stumpp, et al. "Comprehensive analytical model for locally contacted rear surface passivated solar cells." *Journal of Applied Physics* **108**, no. 12, (2010): 124510-124510.
[WUN06]: F. Wünsch, G. Citarella, O. Abdallah, and M. Kunst. "An inverted a-Si: H/c-Si hetero-junction for solar energy conversion." *Journal of non-crystalline solids* **352**, no. 9 (2006): 1962-1966.
[YAN13]: A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, et al, "24.7% Record Efficiency HIT® Solar Cell on Thin Silicon Wafer", *In Proceedings of the 28th EUPVSEC*, Paris, France (2013).
[YAO13]: Yu Yao, John Rodriguez, Jie Cui, Alison Lennon, Stuart Wenham, ""Uniform plating of thin nickel layers for silicon solar cells"", *Energy Procedia*, **38**; (2013): 807 – 815
[ZEM12]: Y. Zemen, T. Prewitz, T. Geipel, et al. "The impact of yield strength of the interconnection on the internal stress of the solar cell within a module." *In Proceedings of the 25th EUPVSEC*, (2010): 4073-4078
[ZHA06]: J. Zhao and A. Wang, "High efficiency rear emitter PERT cells on Cz and FZ n-type silicon substrates." *In Proceedings of the 4th WCPEC*, 1, (2006): 996-999
[ZHA96]: J. Zhao, A. Wang, P. P. Altermatt, et al., "24% Efficient perl silicon solar cell: Recent improvements in high efficiency silicon cell research", *Solar energy materials and solar cells* **41** (1996): 87-99.
[ZHA99]: J. Zhao, A. Wang, and M.A. Green, "24.5% Efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates", *Progress in Photovoltaics: Research and Applications*, **7**, (1999): 471-474

APPENDIX **A**

Specific contact resistance

The contact resistance R_c and the specific contact resistance ρ_c in this work were determined using a measurement technique known as the transfer length method (TLM). Other determination methods have been proposed in literature and are reviewed in the following literature [COH83, SCH84, SCH90, STA09].

As mentioned in Chapter 2.2, a figure of merit for ohmic contacts is the specific contact resistance ρ_c (in $\Omega \cdot cm^2$), also referred to as specific contact resistivity or contact resistivity. The theoretical definition of ρ_c is the reciprocal of the derivative of current density (j) with respect to the voltage (V) at zero bias [SCH84]:

$$\rho_c = \left(\frac{\partial j}{\partial V}\right)^{-1}_{V=0} \tag{A.1}$$

Electrical measurements cannot provide ρ_c directly. The measurements result in a measured contact resistance R_c (in Ω) from which ρ_c is determined using additional theoretical considerations [SCH90].

Several methods have been proposed for measuring the contact resistance. In this thesis, the contact resistance was determined using a measurement technique known as the transfer length method (TLM) as first proposed by Shockley in 1964 [SCH64]. Two TLM test structures exist as shown in Figure A.1. In the original structure (Figure A.1a), also known as ladder structure, the two contacts at the ends of the test structure served as entry and exit point for the current and the voltage drop was measured between one of the large contacts and each of the successive, equally spaced, narrow contacts. Later on, the ladder test structures were improved by making unequally spaced contacts, with the voltage drop measured between adjacent contacts so that no other contacts would interfere with the measurement.

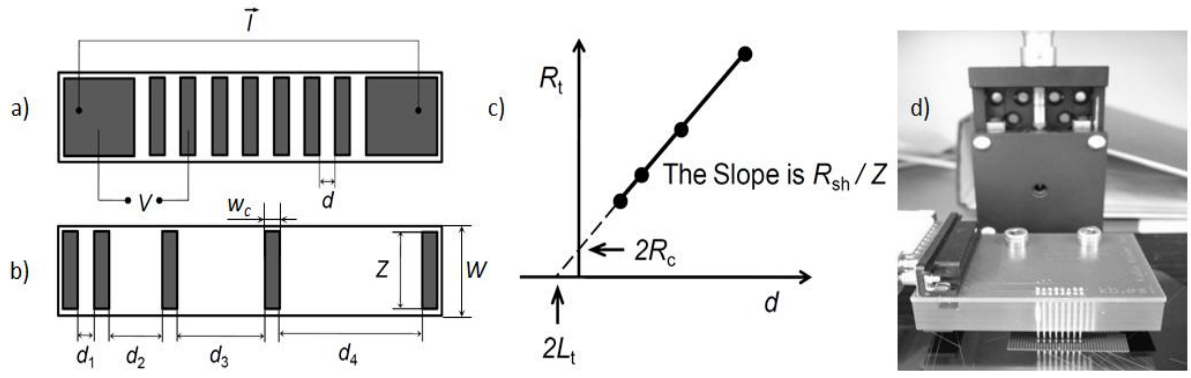


Figure A.1: Top view of transfer length method (TLM) test structures showing the contacts (dark areas) to doped silicon: as originally described by Shockley (a) and with unequal spacing between contacts (b). (c) Plot of the total resistance R_t as function of contact spacing d with L_t the transfer length, R_{sh} the sheet resistance, R_c the contact resistance, and Z the contact length. All drawings are taken from [STA09]. (d) Semi-automated measurement tool from Kb-esi with a TLM test structure (lased diced from a finished solar cell) under test.

Typically, the contacts are made to the front emitter and the current flow from the emitter into the contact can be regarded as lateral flow. The distance at which is current density has dropped by *1/e* from its initial value is defined as the transfer length (L_t), given by:

$$L_t = \sqrt{\rho_c / R_{sh}} \tag{A.2}$$

Using the test structure in Figure A.1b and provided that $Z=W$, the total resistance R_t between any contact is defined as [SCH90]:

$$R_t = \frac{R_{sh}}{Z} d + 2R_c = \frac{R_{sh}}{Z} d + 2 \frac{\rho_c}{L_t Z} \coth\left(\frac{w_c}{L_t}\right) \tag{A.3}$$

which for a contact width $w_c \geq 1.5 L_t$ gives $\coth(w_c/L_t) \approx 1$ and

$$R_t = \frac{R_{sh}}{Z} d + 2R_c \approx \frac{R_{sh}}{Z} [d + 2L_t] \tag{A.4}$$

The total resistance is measured for various contact spacing and plotted versus the contact spacing (d). From the plot in Figure A.1c, using equation (A.4), three parameters can be extracted. Knowing the contact length Z, the emitter sheet resistance R_{sh} can be extracted from the slope, that equals R_{sh}/Z. The intercept at $d = 0$ results in $2R_c$ (contact resistance). The the intercept with the x-axis, at $R_t = 0$, gives $2L_t$ from which ρ_c can be calculated.

The intercept at $R_t = 0$ giving L_t is sometimes not very distinct leading to incorrect ρ_c values. Nevertheless, by measuring the voltage drop between contacts n and n+1 with the current flowing between contacts n-1 and n, the end resistance (R_E) can be determined. Knowing R_c and R_E, an experimental value can for L_t , and hence ρ_c, can be obtained from:

$$L_t = \frac{w_c}{\cosh^{-1}\left(\frac{R_c}{R_E}\right)} \tag{A.5}$$

To increase accuracy, we first started by applying this methodology to TLM structures defined by photolithography patterning and lift-off (see Chapter 5.2.3). To avoid errors due to lateral current spreading, another photolithography step was required to pattern the emitter prior to contact lift-off so that the emitter length (W) would be close to the contact length (Z). However, not only these structures were complicated to define and slow to measure (manual placements of probes) but they were far from the real solar cell device featuring laser ablated contacts. Therefore, most TLM results presented in this thesis were measured using a semi-automated tool from Kb-esi and test samples laser diced from finished solar cells as shown in Figure A.1d. Such test samples are not optimized for contact resistance measurements as contacts are equally spaced and hence interfere with the measurement. Nevertheless, this approach presented several advantages. First, measurement speed was greatly improved giving the possibility to measure many samples per condition and also to measure all combinations of contact pairs within each sample. Second, the effect of annealing on ρ_c was clearly identified as TLM measurements were possible on the same samples prior to and after annealing (see Chapter 5.4.3). Finally, it gave the possibility to create ρ_c maps by measuring TLM samples at various locations within the same solar cell which proved to be useful to identify non-uniformities in ρ_c induced during processing (e.g. emitter formation, plating).

Additional inaccuracies are introduced by the fact that R_{sh} is assumed to be identical under the contacts and between the contacts which might not be the case due to effects of contact formation. Modified expressions have been derived for R_c that take this into consideration [SCH90, MET07]. However, we did not implement these expressions as we already relied on test samples that were non-optimized for contact resistance measurements. Using the semi-automated TLM tool, we found that uncertainties in specific contact resistance values became important below $1x10^{-5}$ $\Omega \cdot cm^2$. Nevertheless, this was sufficient as we only wanted to accurately measure ρ_c values down to $5x10^{-4}$ $\Omega \cdot cm^2$ (see Chapter 4).

In Chapter 2.2, it was mentioned that ρ_c values down to 10^{-8} $\Omega \cdot cm^2$ were possible with NiSi contacts based on literature data. However, the test structures that are required to measure such low values are incompatible with solar cell processing as they rely on planar devices and advanced photolithography patterning. Two different test structures are commonly used. For the first structure shown in Figure A.2a, the measurement technique involves measuring the resistance across silicon fragments interrupted by one, two or n silicided segments and comparing it a reference fragment (not interrupted). As the fragments have been designed to have equal silicided and non-silicided segments lengths, the difference between the reference resistance and the other resistances is attributed to the contact resistance contribution from which the specific contact resistance can be extracted based on theoretical considerations [STA09]. The second test structure is called Cross-Bridge Kelvin Resistor (CBKR) and generally consists of four terminals as shown in Figure A.2b. The measurement technique involves forcing a current (I) between pads 1 and 2 and measuring the voltage drop (V_{34}) between pads 3 and 4 from which ρ_c can be directly extracted. Because the CBKR test structure only involves one contact, there is practically no limitation in the ρ_c value that can be extracted. However, some theoretical considerations are also required to take into account current crowding effects [STA09].

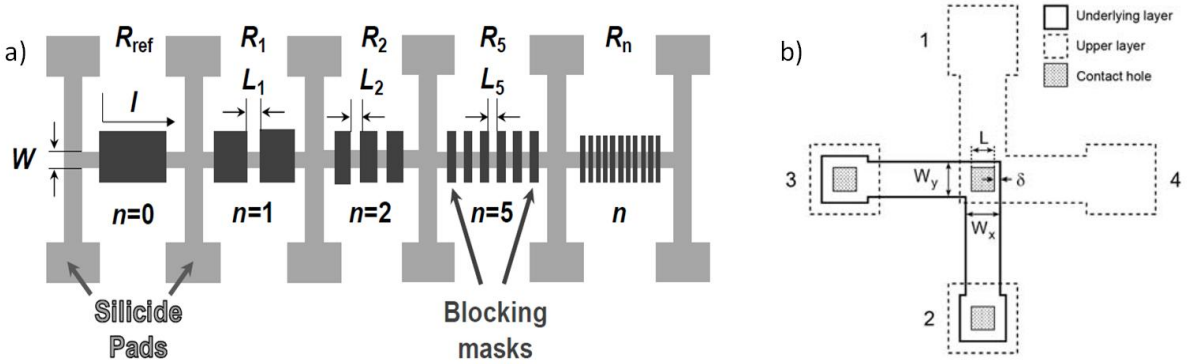


Figure A.2: a) Contact resistance test structures (top view) consisting of a number of silicon fragments. The first fragment is called a reference fragment, not interrupted by silicide segments. Other fragments consist of alternating silicided and unsilicided segments formed by using a silicide-blocking mask. b) Four-terminal Cross-Bridge Kelvin Resistor (CBKR) test structure (top view) with geometry parameters definition. All drawings are taken from [STA09].

APPENDIX **B**

X-ray fluorescence

Deposited metal thicknesses were determined using a table-top X-Ray fluorescence (XRF) tool. The working principle and the advantages of thickness measurement by XRF are quickly discussed here. Further details beyond that can be found in technical literature [SCH90].

In X-ray fluorescence (XRF), primary X-rays incident on the sample are absorbed by ejecting electrons from the atomic K-shell as illustrated in Figure B.1a. Electrons from higher-lying levels, for example the L shell, drop into the K-shell vacancies and the energy liberated in the process is given off as secondary X-rays. XRF is a non-contact, non-destructive method which allows elemental analysis of solids and liquids. It can be used to determine the composition of an alloy or the thickness of multilayer coatings with nm range resolution. It gives the average sample composition over the X-ray absorption depth rapidly, but has no profiling capability. The method is suitable for conductors as well as for insulators, since X-rays are uncharged. It is not a high-resolution method, as X-rays are difficult to focus, but the instrumentation is relatively inexpensive.

The basic structure of an XRF measurement tool is shown in Figure B.1b. A picture of the X-Strata 980 XRF tool (Oxford Instrument) installed at imec in shown in Figure B.1c illustrating the fact that XRF tools can be relatively compact. Primary X-rays are generated in a X-ray tube by bombarding a metal anode with electrons (50 keV acceleration voltage for the X-Strata). A collimator focuses the X-rays onto the test sample. X-ray emission (fluorescence) from both the coating and the substrate materials of the test sample is detected with an energy dispersive detector (EDS) which for the X-strata is a p-i-n silicon diode. Using the appropriate electronics, the charge pulses collected by the p-i-n diode are converted to voltage pulses, amplified, and attributed to the X-ray energy [SCH90]. The X-ray energy identifies the impurity and the intensity can be converted to thickness if the density of the material in the coating is known. Typically, XRF thickness measurements are calibrated by establishing standards of a given coating in which the thickness is measured independently.

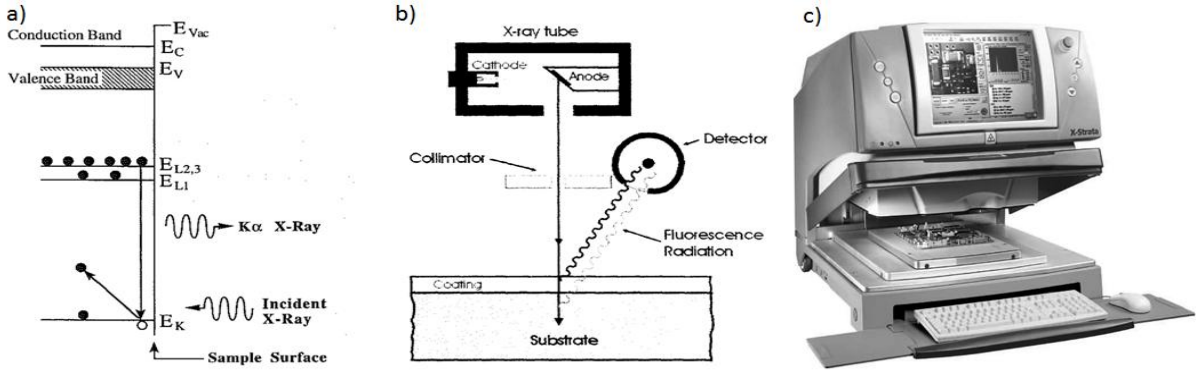


Figure B.1: a) Electronic processes in X-ray fluorescence (XRF) [SCH90], b) Schematic of XRF measurement method [PET01], c) Picture of the X-Strata 980 XRF tool (Oxford Instrument) installed at imec.

Since XRF is subject to a matrix effect, which is the absorption of secondary X-rays by the sample itself, the accuracy of XRF thickness measurements decreases for multilayers. For this reason, XRF thickness measurements that were performed were mainly qualitative. Nevertheless, they proved to be very useful both as process control and to evaluate thickness non-uniformities within wafer and wafer-to-wafer after Ni/Cu/Ag plating. XRF measurements also proved to be ideally suited for a rapid initial survey of the surface (e.g. failure interface after ribbon pull tab, nickel silicide formation after unreacted Ni removal, etc.).

In this work, we also used quantitative XRF thickness measurements of thin Ni layers deposited by bias-assisted light induced plating (LIP) in both busbar and finger areas. Ni standards were created with known thicknesses which were determined by scanning electron microscopy (SEM). Ni density in the XRF tool was adjusted to 8.9 g/cm^3 which is relatively close to the density of pure Ni (9.07g/cm^3) [diB00]. Using this, a good agreement over a wide range of Ni thicknesses was found between SEM and XRF thickness measurements as shown in Figure B.2a. As illustrated in Figure B.2b, the diameter D_{XRF} of the XRF collimator is much smaller than the finger width w_c and hence a correction factor R had to be applied to accurately determine Ni thickness by XRF in the finger areas which is given by:

$$R = \frac{\pi \cdot (D_{XRF})^2}{4} \frac{1}{w_c \cdot D_{XRF}} = \frac{\pi \cdot D_{XRF}}{4 w_c} \tag{B.1}$$

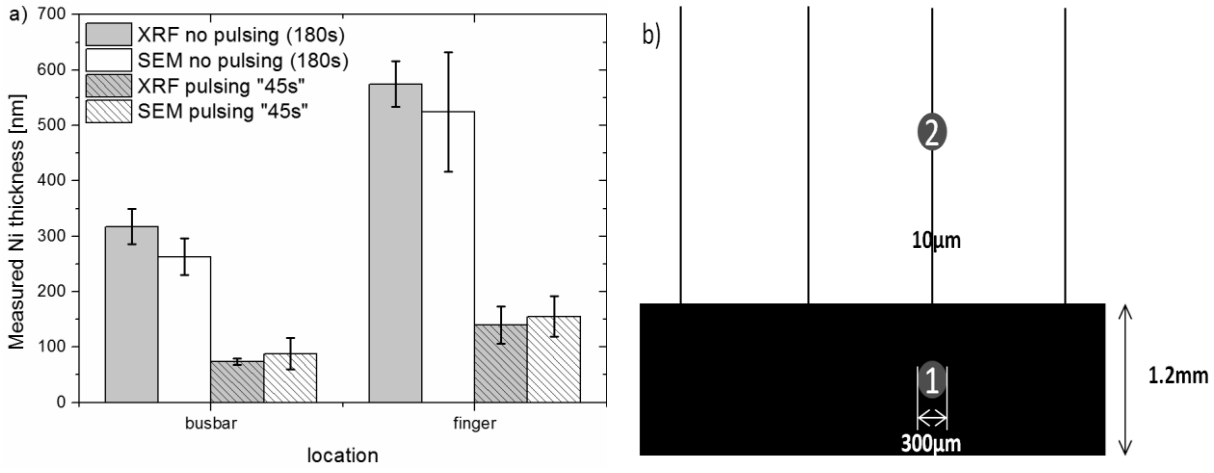


Figure B.1: a) X-ray fluorescence (XRF) and scanning electron microscopy (SEM) thickness measurements in busbars and fingers of Ni layers deposited by bias-assisted light-induced plating. This figure was further discussed in Chapter 9.1. b) Schematic of XRF thickness measurement in busbar area (number 1) and in finger area (number 2) using a XRF collimator diameter of 300µm.

APPENDIX C

DOE matrices

Design of experiments (DOE) matrices and sorted parameter estimates given here were obtained using the software JMP and were used in Chapter 7.2.3 to evaluate the influence of cell processing on adhesion results. All conditions in DOE matrices are repeated four times.

Table C.1: ½ factorial with center points DOE matrix for ps-UV laser ablated samples and Ni deposited by sputtering. Laser pulse energies in % correspond to mean laser powers of 65, 85, and 100mW respectively.

label	Pattern	Ni [nm]	Sinter temp [˚C]	Sinter time [sec]	laser pulse energy [20,25,30%]	laser pulse overlap [0,25,50%]
L1	−−−−+	40	275	30	-1	1
L2	−−−+−	40	275	30	1	-1
L3	−−+−−	40	275	90	-1	-1
L4	−−+++	40	275	90	1	1
L5	−+−−−	40	325	30	-1	-1
L6	−+−++	40	325	30	1	1
L7	−++−+	40	325	90	-1	1
L8	−+++−	40	325	90	1	-1
L9	00000	100	300	60	0	0
L10	00000	100	300	60	0	0
L11	00000	100	300	60	0	0
L12	+−−−−	160	275	30	-1	-1
L13	+−−++	160	275	30	1	1
L14	+−+−+	160	275	90	-1	1
L15	+−++−	160	275	90	1	-1
L16	++−−+	160	325	30	-1	1
L17	++−+−	160	325	30	1	-1
L18	+++−−	160	325	90	-1	-1
L19	+++++	160	325	90	1	1

Table C.2: Full factorial with center points DOE matrix for wet etched samples (photolithography patterning).

LABEL	Pattern	Ni [nm]	Sinter temp [˚C]	Sinter time [sec]
WE1	−−−	40	275	30
WE2	−−+	40	275	90
WE3	−+−	40	325	30
WE4	−++	40	325	90
WE5	000	100	300	60
WE6	000	100	300	60
WE7	+−−	160	275	30
WE8	+−+	160	275	90
WE9	++−	160	325	30
WE10	+++	160	325	90

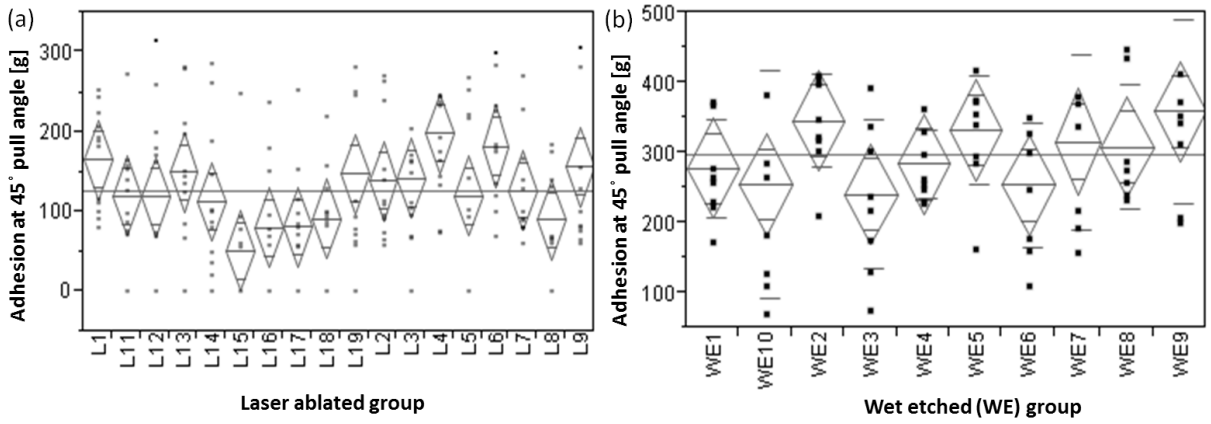


Figure C.1: Measured adhesion values at 45˚ pull angle for a) laser ablated samples and b) wet etched samples.

Term	Contrast	Lenth t-Ratio	Individual p-Value
Ni um	-19.3885	-3.08	0.0036*
laser pulse overlap	19.4364	3.08	0.0035*
Sinter temp	-9.5322	-1.51	0.1316
laser pulse energy	4.6693	0.74	0.4633
Sinter time	-4.4377	-0.70	0.4846
Ni um*Ni um	-4.2718	-0.68	0.5006
Ni um*laser pulse overlap	-1.9271	-0.31	0.7594
Ni um*Sinter temp	5.6282	0.89	0.3712
laser pulse overlap*Sinter temp	-1.2615	-0.20	0.8402
Ni um*laser pulse energy	-1.5991	-0.25	0.7977
laser pulse overlap*laser pulse energy	17.8899	2.84	0.0058*
Sinter temp*laser pulse energy	4.8753	0.77	0.4423
Ni um*Sinter time	1.3587	0.22	0.8285
laser pulse overlap*Sinter time	5.5288	0.88	0.3805
Sinter temp*Sinter time	3.6301	0.58	0.5687
laser pulse energy*Sinter time	-3.1016	-0.49	0.6296

Figure C.2: Sorted parameter estimates for adhesion of laser ablated samples.

Term	Contrast	Individual p-Value
Sinter temp	-12.1508	0.2936
Ni um	9.9375	0.3875
sinter time	-0.1469	0.9896
Sinter temp*Sinter temp	2.0823	0.8555
Sinter temp*Ni um	9.9612	0.3864
Sinter temp*sinter time	-13.9045	0.2315
Ni um*sinter time	-25.0366	0.0354*
Sinter temp*Ni um*sinter time	-8.0054	0.4894

Figure C.3: Sorted parameter estimates for adhesion of wet etched samples.

Term	Contrast	Individual p-Value
Sinter temp	-0.138451	0.2149
Sinter time	-0.095455	0.3841
Ni um	0.037597	0.7400
laser pulse energy	-0.033934	0.7645
pulse overlap	0.013044	0.9084
Sinter temp*Sinter temp	-0.025157	0.8216
Sinter temp*Sinter time	0.004101	0.9715
Sinter temp*Ni um	0.064776	0.5733
Sinter time*Ni um	0.075497	0.4903
Sinter temp*laser pulse energy	-0.058504	0.6120
Sinter time*laser pulse energy	-0.064036	0.5771
Ni um*laser pulse energy	-0.059586	0.6053
Sinter temp*pulse overlap	0.121281	0.2743
Sinter time*pulse overlap	0.039026	0.7315
Ni um*pulse overlap	0.010512	0.9257
laser pulse energy*pulse overlap	0.119885	0.2790

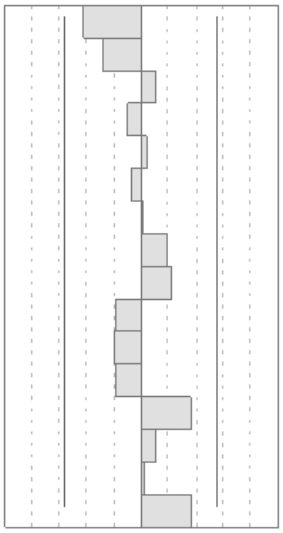


Figure C.4: Sorted parameter estimates for pseudo fill factor (pFF) of laser ablated samples.

Term	Estimate	Std Error	t Ratio	Prob>|t|
sinter temp(275,325)	-2.779642	0.85194	-3.26	0.0028*
Ni um*sinter time	2.6108925	0.85194	3.06	0.0047*
sinter temp*sinter time	-2.275962	0.852253	-2.67	0.0123*
Ni um(40,160)	2.1572115	0.852253	2.53	0.0170*
sinter time(30,90)	-1.967788	0.852253	-2.31	0.0283*

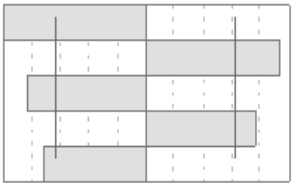


Figure C.5: Sorted parameter estimates for pseudo fill factor (pFF) of wet etched samples.

Curriculum Vitae

August 2nd, 1986	Born in Morlaix, France
2004-2006	Preparatory school to French Grandes Ecoles at ISEP (Paris, France) (2nd year final ranking: 1st/48– 1st year final ranking: 3rd/52).
2006-2009	Bachelor and Master in Materials Science & Engineering at INSA (Lyon, France) (Magna cum laude).
2007-2009	Master in Electrical and Process Engineering at University of Lyon (Lyon, France) (Magna cum laude, 2nd/35).
2010-2014	PhD research in Electronic Engineering at KU Leuven (Leuven, Belgium) in collaboration with imec (Leuven, Belgium).
January 2014	PhD defense: "Nickel/copper plated contacts as an alternative to silver screen printing for the front side metallization of industrial high efficiency silicon solar cells".